AN11706

PN7462AU Antenna design guide

Rev. 1.0 — 9 March 2016
336910

Application note
COMPANY PUBLIC

Document information

Info	Content
Keywords	PN7462AU, Antenna design
Abstract	This document describes the antenna design related to the PN7462AU.

Revision history

Rev	Date	Description
1.0	20160309	Initial version

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1. Introduction

The antenna design for the PN7462AU is not much different than the antenna design for most of the other NXP reader ICs in general. However, some PN7462AU specific details need to be considered to get an optimum performance.

This document describes the generic NFC and RFID antenna design rules in section 3 as simple as possible, considering the different requirements due to ISO/IEC 14443, NFC or EMVCo as introduced in section 2.

The section 4 describes the antenna design for the PN7462AU in detail.

In the Annex in section 5 some basics about the antenna impedance measurement and the related tools can be found.

2. NFC Reader antenna design

For the NFC operation three different communication modes are specified in [4]:

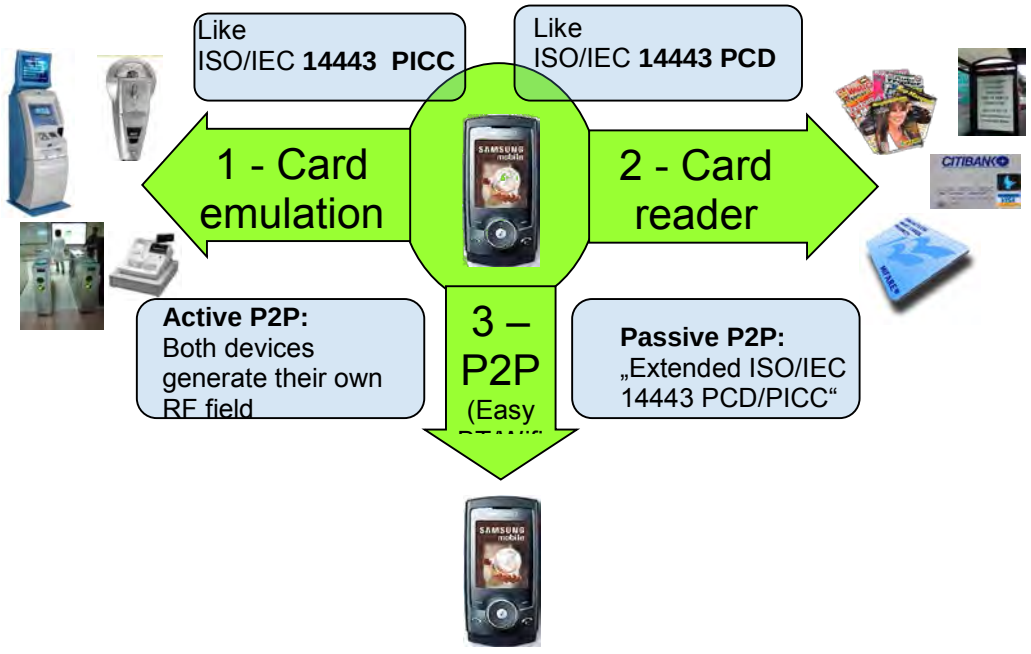
1. In the **card emulation mode (CM)** the NFC device can be used in (existing) NFC reader infrastructure. In the CM the NFC device behaves in principle like a PICC, as defined in [2]. This mode is optional.
2. In the **card reader mode (RM)** the NFC device can be used with (existing) NFC cards. In the RM the NFC device behaves in principle like a PCD, as defined in [2]. This mode is mandatory.
3. In the **peer to peer mode (P2P)** the NFC device can communicate to other NFC devices, either being the initiator, starting the communication, or being the target, answering the communication.

The Fig 1 shows the NFC device in the centre, offering all three NFC communication modes. For the communication between two NFC devices the two different P2P modes are available:

1. **Active P2P**: Both NFC devices, the initiator as well as the target, are required to generate their own magnetic field, when sending data. This mode is optional.
2. **Passive P2P**: The initiator always generates the magnetic field, while the target uses the load modulation principle to send its data. This mode is mandatory.

In this document only the analog topics are discussed, which are relevant for the antenna design. Neither the digital protocol nor the advantages/disadvantages for different use cases are content of this document.

For the optimization of the performance it might makes sense to restrict the functionality to only one or two of the communication modes.



(1) ISO/IEC 14443 PICC and PCD here just indicate the similarity of the communication but do not automatically mean interoperability.

(2) “Extended ISO/IEC14443 PCD/PICC” simply refers to the antenna design parameters and does not include the protocol.

Fig 1. NFC communication modes

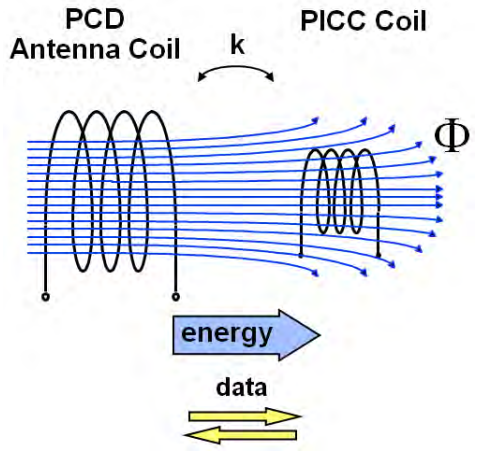
2.1 ISO/IEC 14443 specifics

The ISO/IEC 14443 (called “ISO” in the following, details see [2]) specifies the contactless interface as widely being used with contactless smartcards like e.g. MIFARE cards.

The ISO/IEC 14443 defines the communication between a reader (“proximity coupling device” = PCD) and a contactless smartcard (“proximity chip card” = PICC). In four parts it describes the physical characteristics (i.e. the size of the PICC antennas), the analog parameters like e.g. modulation and coding schemes, the card activation sequences (“Anticollision”) and the digital protocol. The ISO/IEC 10373-6 (see [3]) describes as well the test setup as well as all the related tests for cards and the reader.

The ISO/IEC 14443 reader antenna consists of an antenna coil, which is matched to the reader IC. This antenna coil, as shown in Fig 2,

1. generates the magnetic field to provide the power to operate a card (PICC),
2. transmits the data from the reader (PCD) to the card (PICC), and
3. receives the data from the card (PICC) to the reader (PCD).

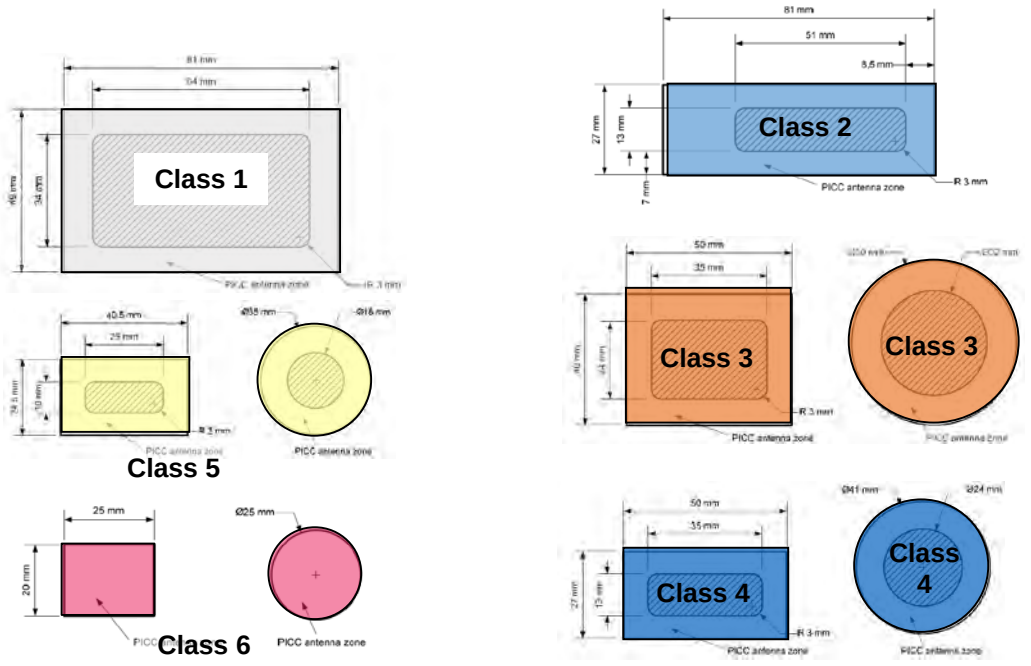


(1) k = coupling coefficient
(2) Φ = magnetic flux

Fig 2. Magnetic coupling between reader (PCD) and card (PICC)

According to the ISO/IEC 14443 the PICC antenna coils can be categorized into the classes 1 …6, as shown in Fig 3.

The PCD antenna is not defined as such, but the PCD must support the classes 1, 2, and 3. The support of the classes 4, 5, and 6 is optional.



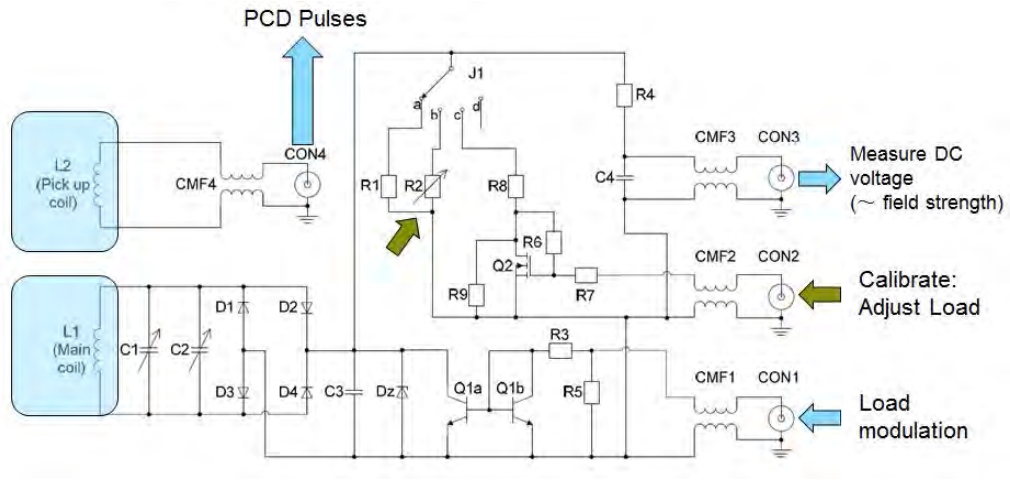
(1) A PCD must always support the classes 1, 2, and 3.

Fig 3. PICC Classes according to the ISO/IEC 14443

The PCD antenna coil sizes are not specified. So for ISO/IEC 14443 compliant readers all different sizes of antenna coils from a few 10 mm^2 up to 20cm diameter can be found in various shapes.

The ISO/IEC 14443 does not specify an operating volume. The reader manufacturer needs to guarantee that within the operating volume - that he himself defines - all related ISO/IEC 10373-6 tests can be passed.

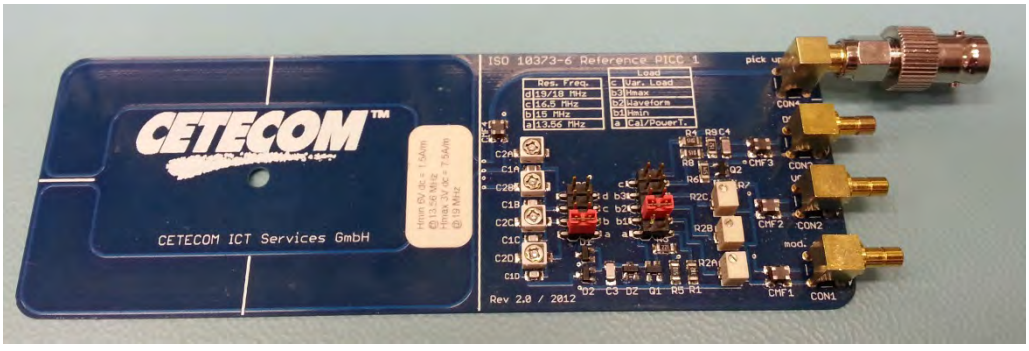
The compliance tests require calibrated ReferencePICCs, as defined in ISO/IEC10373-6. The schematic of such ReferencePICC is shown in Fig 4. For each PICC Class there is one Reference PICC, which needs to be calibrated according to the required measurement. Practically it makes sense to use one calibrated ReferencePICC for each measurement case.



(1) Details see [3].

Fig 4. ISO/IEC 10373-6 ReferencePICC

Some ReferencePICCs, which are commercially available (e.g. Fig 5), are pre-calibrated and equipped with several jumper options to address the most relevant tests with a single ReferencePICC.



(1) The jumper settings allow different pre-calibrations.

Fig 5. ISO/IEC 10373-6 Reference PICC Class 1

Still for each PICC Class a separated ReferencePICC is required.

The **most** relevant analog tests for PCDs are:

1. Field strength test (min and max)
2. Wave shape tests (for all bit rates)
3. Load modulation amplitude tests

Note: This application note does not replace the detailed test description in the ISO/IEC 10373-6.

There is no common certification process for ISO/IEC14443 compliance in place, even though many national bodies use the ISO/IEC 14443 to operate the electronic passports and electronic ID cards. For these programs some nations have established a certification process to guarantee interoperability. An example is given in [5].

2.1.1 Field strength tests

For the field strength test it is preferred to have the PCD send a continuous carrier, i.e. it performs no modulation.

The field strength tests simply require the calibrated ReferencePICC and a dc voltage measurement device (volt meter or oscilloscope). The field strength is equivalent to the calibrated (and required) voltage level. The ISO/IEC 10373-6 defines minimum voltage levels, corresponding to the minimum required field strength, and maximum voltage levels, corresponding to the maximum allowed field strength. The measured voltage levels must stay in between these limits.

2.1.2 Wave shape tests

The PCD needs to send the related pulse(s): It may send a ISO/IEC 14443 REQA and / or REQB with the required bit rate, as e.g. specified in [5]. Any other command fits the purpose, too.

Note: For the test of higher bit rates it makes sense to implement some specific test commands, which send artificial commands, e.g. REQA and / or REQB, using the coding and modulation of the corresponding higher bit rates. The standard way of activating higher bitrates cannot be applied, since the ReferencePICC for ISO/IEC 14443-2 tests does not allow the protocol layer, which is normally required to switch to higher bit rates.

The wave shape tests require

1. a calibrated ReferencePICC, which is placed at the position of the calibrated field strength (corresponding to the dc voltage as measured in section 2.1.1),
2. a digital oscilloscope with a measurement bandwidth of 500Msamples or higher, and
3. a tool that filters and transforms the oscilloscope data into the envelope signal according to the ISO/IEC 10373-6.

The tool normally returns the filtered and transformed envelop as well as the corresponding values of rise and fall times, residual carrier levels and over- and undershoots, which must be kept within the given limits.

2.1.3 Load modulation tests

The PCD needs to send a teat command, which allows to check a response from the ReferencePICC.

The load modulation tests require

1. a calibrated ReferencePICC, which is placed at the position of the calibrated field strength (corresponding to the dc voltage as measured in section 2.1.1),

2. a signal generator with a pattern generator, that provides the load modulation signal as a response to the PCD test commands.

The response must be triggered by the PCD test command, i.e. the signal generator needs a delayed trigger input either from the field or from the PCD itself. The voltage level of the load modulation input signal for each test case must be (pre-) calibrated in the TestPCD set up.

The PCD must be able to receive all the responses with the given minimum load modulation signal level.

2.2 EMVCo specifics

EMVCo specifies a contactless interface for point of sales (POS) terminals (= PCD) and the corresponding contactless payment cards in [6]. This interface is very similar to the one defined ISO/IEC 14443, but it uses its own set of requirements and specification details. The EMVCo test equipment and way of testing is quite different from the test specification as defined in ISO/IEC 10373-6.

For the reader tests a calibrated EMVCo Reference PICC is required. This Reference PICC can be bought only from one of the accredited labatories.

Some of the antenna design parameters also need to be adapted towards EMVCo requirements.

The **most** relevant analog tests for PCDs are:

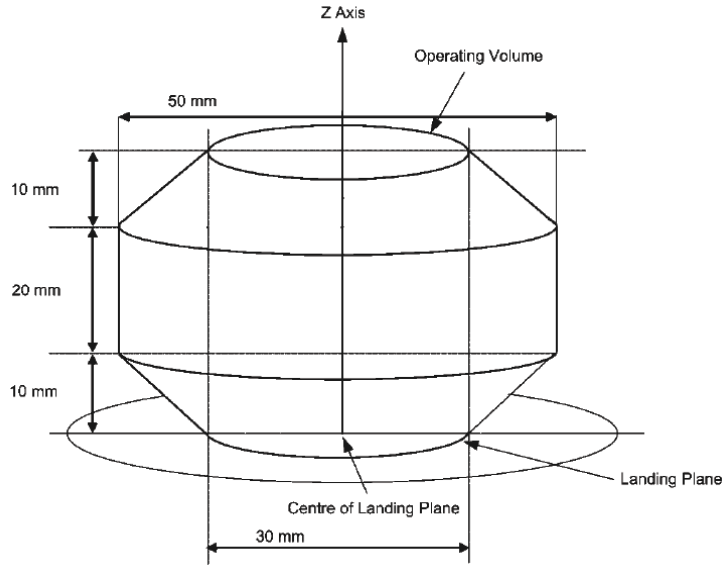
1. PCD power test (field strength)
2. Modulation PCD-> PICC tests (wave shape tests)
3. Load modulation tests

EMVCo specifies and requires only the bit rate of 106kbit/s for both type A and B, but no higher bit rates.

Note: This application note does not replace the detailed test description in the ISO/IEC 10373-6.

2.2.1 EMVCo Operating volume

One main difference for the tests is the definition of an operating volume, as shown in Fig 6. This volume is tested with the EMV-Test-PICC.



(1) Details see [6].

Fig 6. EMVCo POS operating volume requirement

Within this volume the given parameters need to be fulfilled.

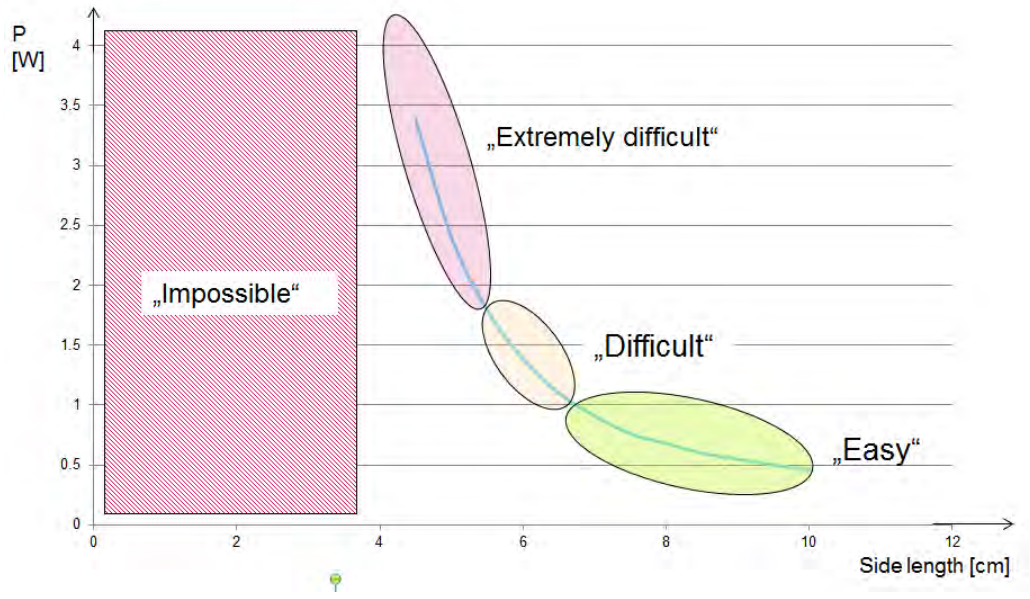
2.2.2 EMVCo Field strength

For the field strength test it is preferred to have the PCD send a continuous carrier, i.e. it performs no modulation.

The voltage level which can be measured in all of the given positions needs to be between the minimum and maximum limit, as given in [6].

Due to the operating volume it can become challenging to meet the EMVCo requirements with small antennas.

The Fig 7 shows the required power versus antenna size. The curve is based on a antenna simulation, which uses a few simplifications, so it does not take the loading effect of the EMVCo Reference PICC into account. On the other the simulation was done under ideal environmental conditions, i.e. no metal environment influences the antenna. The simulation results can be taken as reference to estimate the design effort especially for small antennas compared to “normal” antenna sizes.



(1) Side length of a square antenna.

(2) These simulation results do neither take any specific environment nor loading effects into account.

Fig 7. EMVCo POS Reader antenna size

2.2.3 EMVCo Wave shapes

The PCD needs to send the related pulse(s): It may send an EMVCo REQA and / or REQB.

The wave shape tests require

1. a calibrated EMVCo ReferencePICC, which is placed at each of the given position (see Fig 6),
2. a digital oscilloscope with a measurement bandwidth of 500Msamples or higher, and
3. a tool that filters and transforms the oscilloscope data into the envelope signal according to the EMVCo test requirement.

The tool normally returns the filtered and transformed envelop as well as the corresponding values of rise and fall times, residual carrier levels and over- and undershoots, which must be kept within the given limits.

2.2.4 EMVCo Load modulation

The PCD needs to send a test command, which allows to check a response from the ReferencePICC. Typically the EMVCo loop back command sequence is used for this.

Note: Since these tests do not replace the certification tests as required by EMVCo, simple tests commands might be even more useful than the full EMVCo test sequence. Such a simple test command can be easily debugged and typically allows an easier triggering.

The load modulation tests require

1. a calibrated ReferencePICC, which is placed at each of the given position (see Fig 6),
2. a signal generator with a pattern generator, that provides the load modulation signal as a response to the PCD test commands.

The response must be triggered by the PCD test command, i.e. the signal generator needs a delayed trigger input either from the field or from the PCD itself. The voltage level of the load modulation input signal for each test case must be set according to [6].

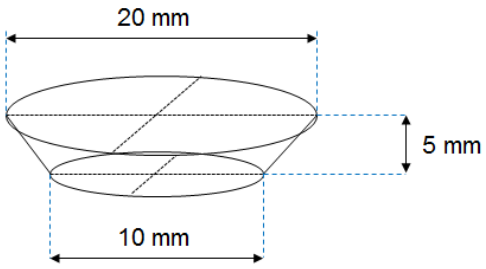
The PCD must be able to receive all the responses with the given minimum load modulation signal level.

2.3 NFC specifics

The standard NFC device needs to fulfill the reader mode (PCD), the passive target and the passive initiator. The passive target from an antenna point of view is very similar to the optional card mode (PICC).

2.3.1 NFC Operating volume

The NFC Forum specifies an operating volume as shown in Fig 8.



(1) Details see NFC Analog Technical Specification, [4]

Fig 8. NFC Forum operating volume

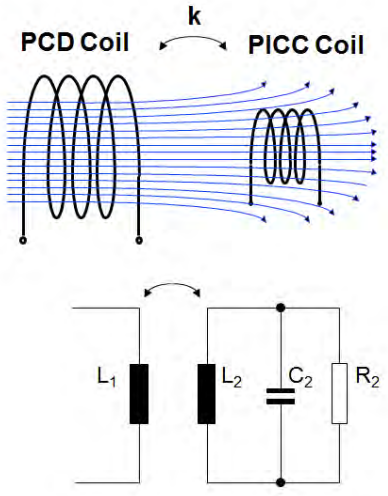
3. Generic PCD antenna design rules

Some of the design rules are very common for NXP NFC Reader designs, i.e. they do neither specifically depend on the used standard (ISO, NFC or EMVCo) nor depend on the NXP Reader IC but rather on physical or technical basics.

3.1 Optimum Antenna Coil

The optimum antenna coil size for a standard PCD can be derived from the Biot-Savart law. The major prerequisites are some simplifications like the assumption that the antenna system is optimized based on the parallel operation of smart cards on top of the PCD antenna. The optimization is derived for the operating distance, i.e. the target is to show the optimum PCD antenna size for a given required operating distance.

The principle and simplified electrical circuit is shown in Fig 9.



(1) Index 1: PCD
(2) Index 2: PICC

Fig 9. PCD Antenna coil

The index 2 indicates the parameters of the PICC. Here the PICC is taken as given, i.e. the parameters with the index 2 cannot be modified. This is another simplification, but also refers to the reality, where the reader antenna optimization does not allow to change card parameters.

The PCD antenna is taken as a circular antenna to allow a simple calculation. The impact of different form factors is discussed later.

Out of this law the coupling coefficient *k* between PCD and PICC antenna can be described as following:

$$k = \mu_0 \cdot \frac{r^2}{2(r^2 + x^2)^{3/2}} \cdot \frac{A_2}{\sqrt{L_{01} \cdot L_{02}}} \quad (1)$$

A_2 = Card antenna coil area, fixed

L_{02} = Card antenna coil single turn inductance, fixed

L_{01} = Reader coil single turn inductance

r = Reader Antenna coil radius

x = Operating distance in the center of the Reader antenna

μ_0 = relative permeability

The single turn inductance can be described like this:

$$L_{01} \approx \frac{2 \cdot 10^{-7}}{[m]} \cdot 2\pi \cdot r \cdot \ln\left(\frac{2\pi \cdot r}{d}\right) \quad (2)$$

d = coil wire diameter with $d << r$

Note: The formula to calculate the inductance of the antenna coil can only be taken as reference. In real life many details influence the result, which are not taken into account in this simple formula. So a measurement of the coil parameters as described below is required anyway.

3.1.1 Number of turns

Changing the number of turns does not change the coupling, since the inductance itself has no influence on the coupling. So in principle antenna coils with a single turn can be used as well as antenna coils with many turns.

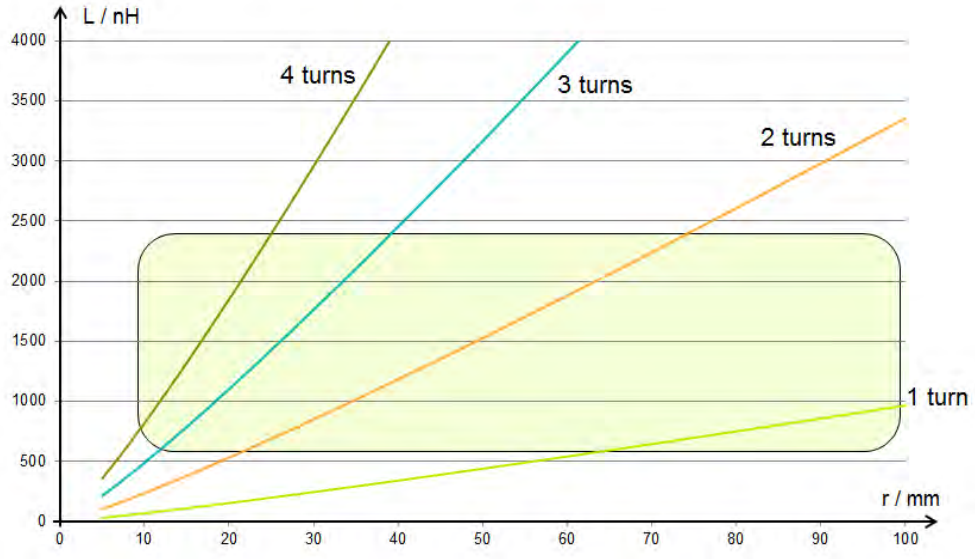
The only remaining parameter to optimize the coupling is the antenna radius r (i.e. the antenna size), and will be discussed in section 3.1.2.

However, the number of turns changes the inductance which on one hand changes the matching circuit.

Out of experience it turns out to be optimum to have an inductance around L ≈ 1µH for a proper matching, but a wide range of L ≈ 300nH up to L≈ 4µH still can be matched properly, so typically 1 up to 4 turns in the normal range of antenna sizes are used.

The Fig 10 shows the typical inductance values versus the antenna coil radius for 1, 2, 3 and 4 turns. These values are just examples, since the environment, the track width or wire thickness and some other parameters may influence the inductance.

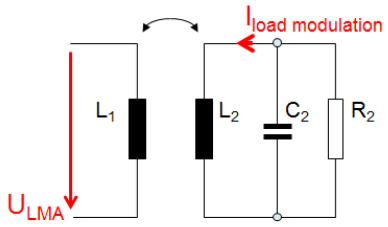
Furthermore the typical PCD antenna coil does not use the circular shape, but rather a rectangular form factor. The given calculated values show the wide range that can be used, and shall be used as reference only. The antenna coil inductance must be measured anyway later on to do the antenna matching.



(1) Green area: target area for standard antenna matching.

Fig 10. Inductance examples versus coil radius

On the other hand the number of turns defines the relationship of voltage level versus current level. Especially for the load modulation (see Fig 11) it might be helpful to increase the number of turns on the PCD antenna coil.



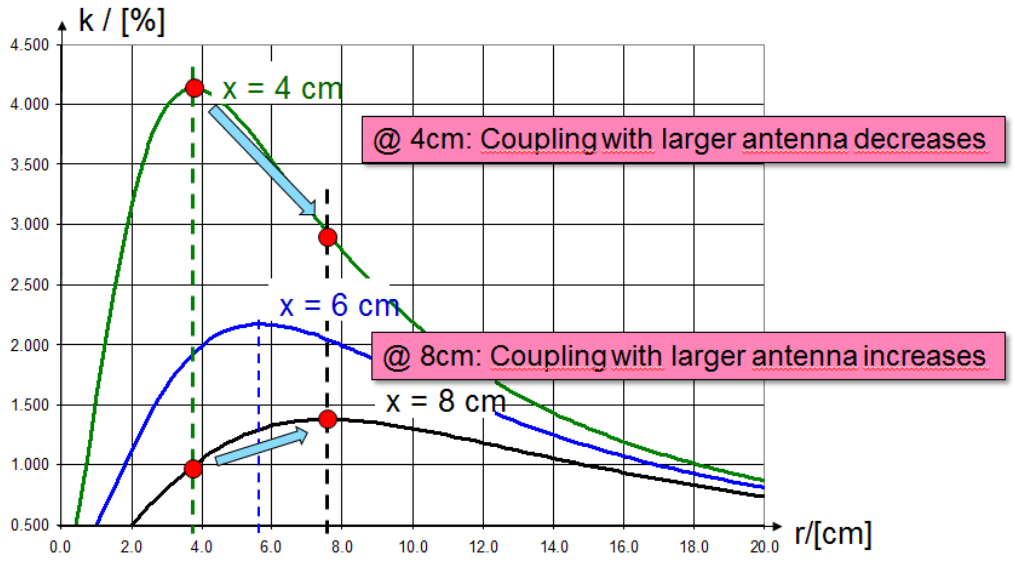
(1) Index1 = PCD

(2) Index 2 = PICC antenna coil

Fig 11. Load modulation

3.1.2 Optimum antenna coil size

Fig 12 shows the coupling coefficient versus antenna radius for three different operating distances. The scaling of the coupling coefficient does not necessarily show the correct absolute value, since some of the fixed parameters are estimated only for this graph. However, the relative value is important to indicate the optimum antenna size.



(1) Green: at a distance of x = 4 cm

(2) Blue: at a distance of x = 6 cm

(3) Black: at a distance of x = 8 cm

(4) The coupling coefficient scaling in this diagram is relative only. The absolute value might differ.

Fig 12. Coupling coefficient vs PCD antenna radius

The maximum coupling can be achieved, when

$$r = x \tag{3}$$

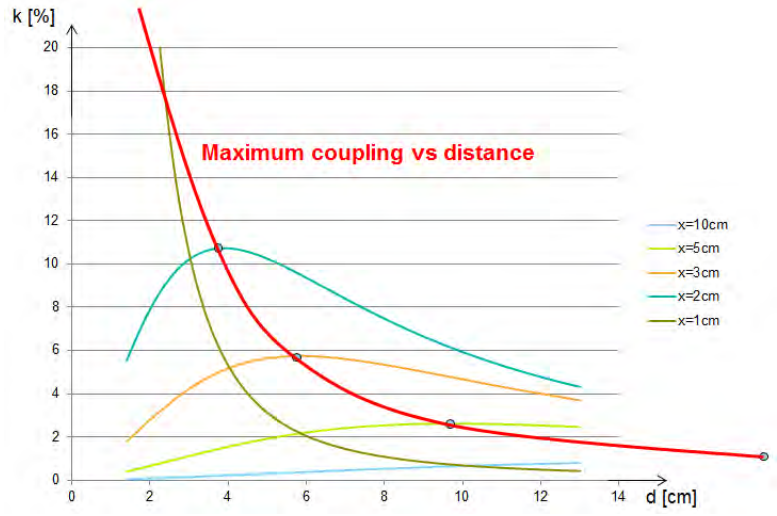
r = Reader Antenna coil radius

x = Operating distance in the center of the Reader antenna

The maximum coupling at an operating distance of 4cm can be achieved with an antenna coil of approximately 4cm radius (i.e. 8cm diameter). Increasing the antenna radius from 4cm to 8cm decreases the coupling at 4cm distance (green curve), but increases the coupling at 8cm distance (black curve).

However, the optimum antenna size as such does not guarantee that the coupling is strong enough.

The maximum coupling coefficient versus the operating distance can be estimated as shown in Fig 13. This maximum coupling is related to the optimum antenna size.



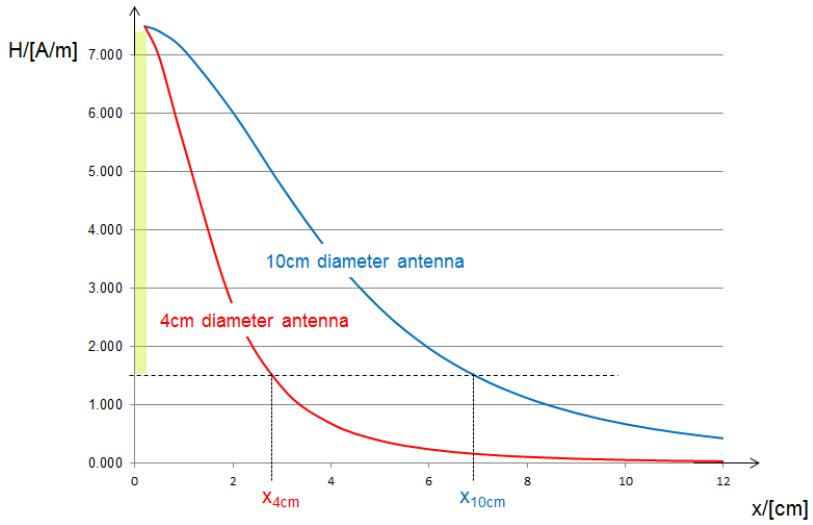
(1) The absolute scale of k might not be correct due to simplifications.

Fig 13. Maximum coupling vs antenna size

Theoretical example:

The Fig 14 shows the field strength versus operating distance of two different antenna sizes. For both antennas the antenna current is tuned to deliver the maximum allowed field strength of 7.5 A/m at the minimum operating distance of 2mm.

The small antenna with 4cm diameter achieves an operating distance of almost 3cm, the large antenna with 10cm diameter achieves an operating distance of almost 7cm.



(1) Minimum required field strength Hmin = 1.5A/m

(2) Both antennas scaled to deliver Hmax = 7.5 A/m at maximum

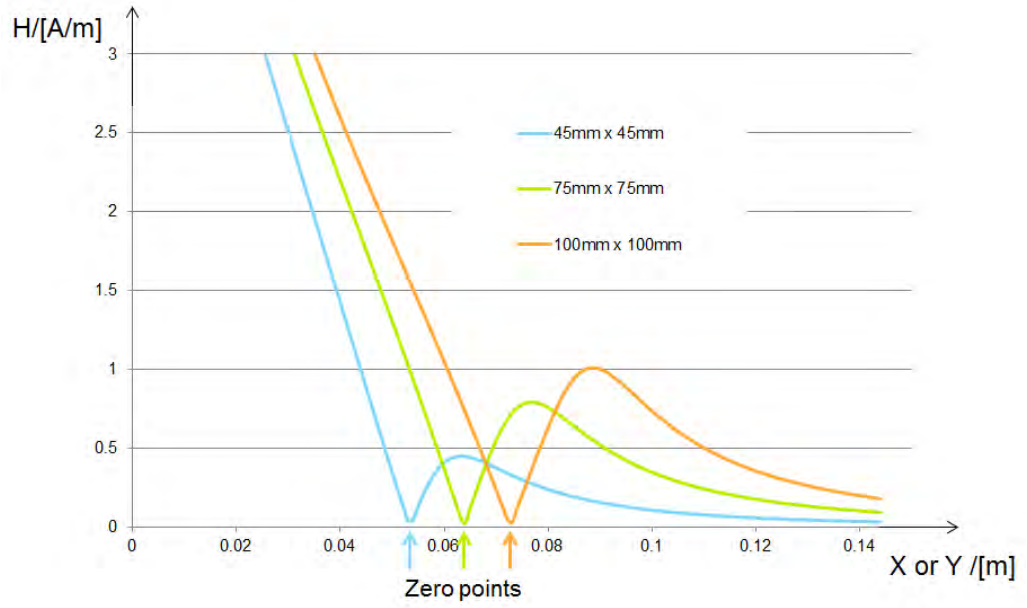
Fig 14. Operating distance x versus antenna size

Note: The large antenna is driven with a current $I_{largeantenna} \approx 4x\ I_{smallantenna}$.

Note: This graph does not include the detuning and loading effect of the reader antenna.

The Fig 15 shows the simulation result of three different square antennas. The magnitude of the field strength is shown versus the distance from the center of the antenna area in either X or Y direction. The curves indicate the zero points, which are areas around the antenna slightly outside the antenna area, where no field can be measured (i.e. where the coupling is zero).

At a zero point no tag device can be operated, even if the required field strength is very low. This needs to be considered, if there is a requirement to read tags within a certain given operating volume, which might touch the zero points, especially if the antenna is too small.



(1) Operating distance = 1cm, X and Y = horizontal distance from antenna center.

(2) These simulation results do neither take any specific environment nor loading effects into account

Fig 15. Magnitude of field strength in 1 cm distance

Note: The field strength is not the same for all three antennas, but has been adjusted individually to achieve the maximum allowed field strength for each antenna.

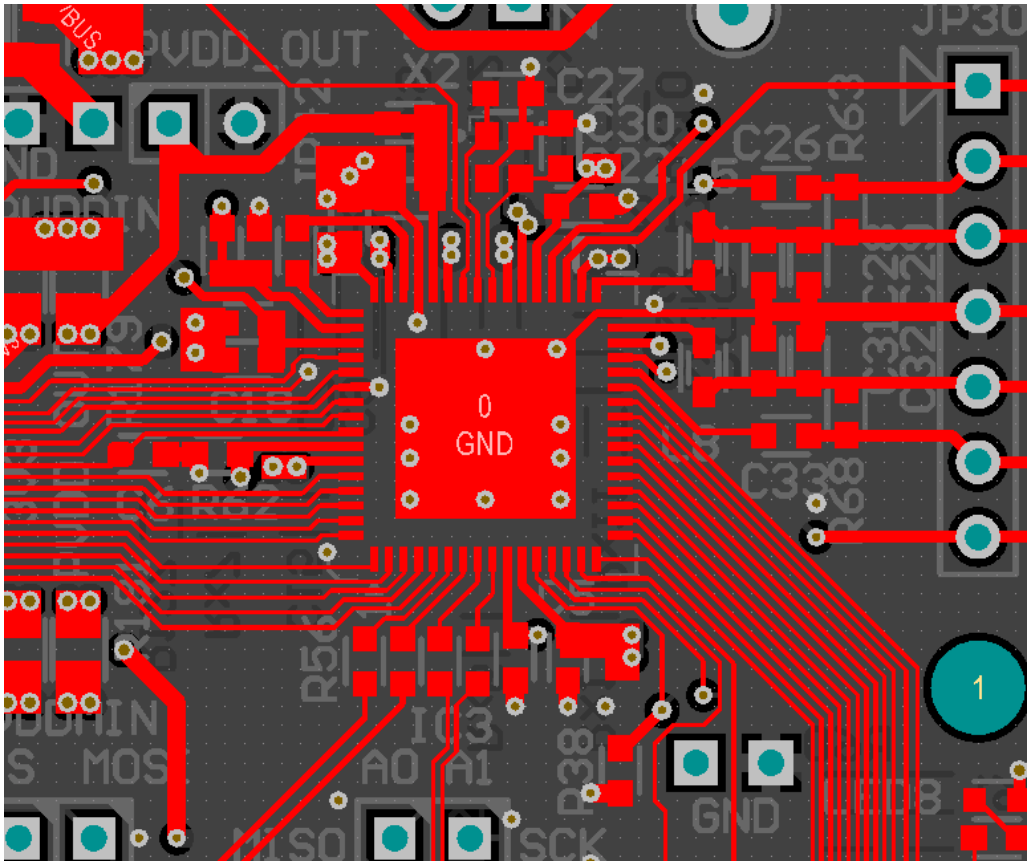
3.2 Layout recommendations

The connection between the TX output pins (TX1 and TX2) and the EMC low pass filter has to be as short as possible. The GND connection especially between TVSS and the C0A and C0B (see Fig 18) capacitors must be as short as possible.

The connection between the block capacitors and the VDD pins need to be as short as possible. This holds especially for the TVDD and its block capacitor.

The PN7462AU evaluation board and its related description (see [8]) can be taken as a reference.

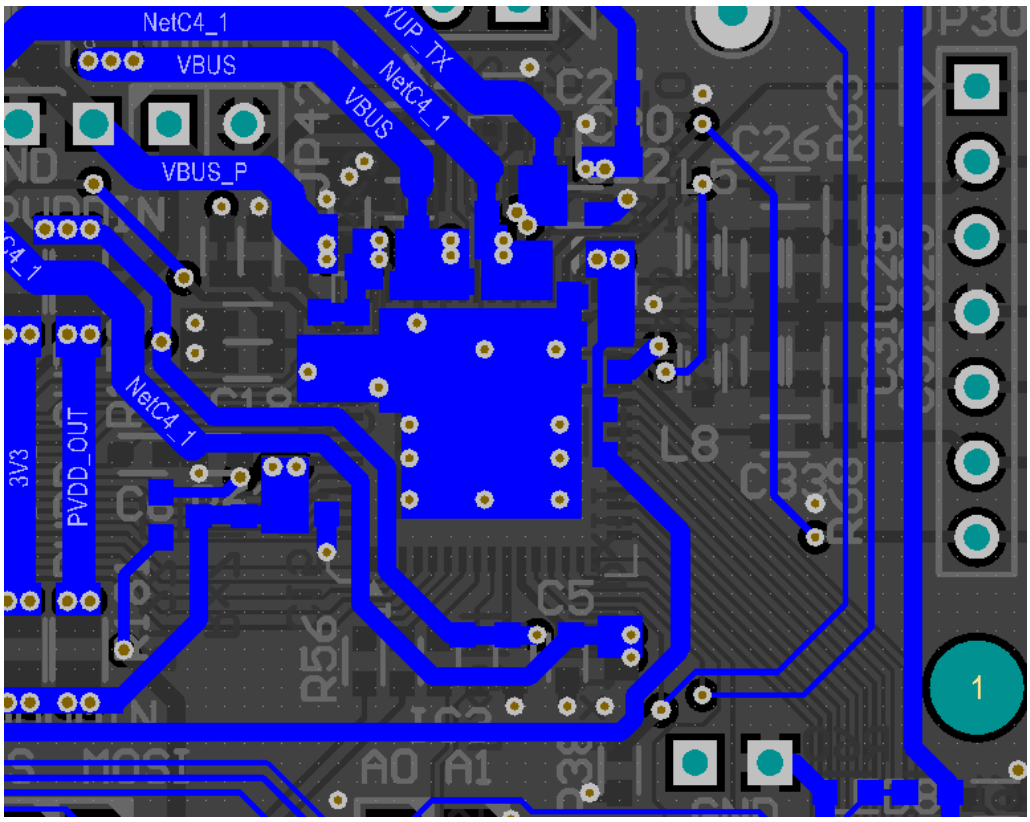
The Fig 16 and Fig 17 show a part of the top and bottom layer structure around the PN7462AU as reference. The GND layer is a complete area of one of the middle layers (not shown).



(1) Part of the top layer

(2) Middle Layer = GND area

Fig 16. PN7462AU Layout Reference Board Top layer



(1) Part of the bottom layer

(2) Middle Layer = GND area

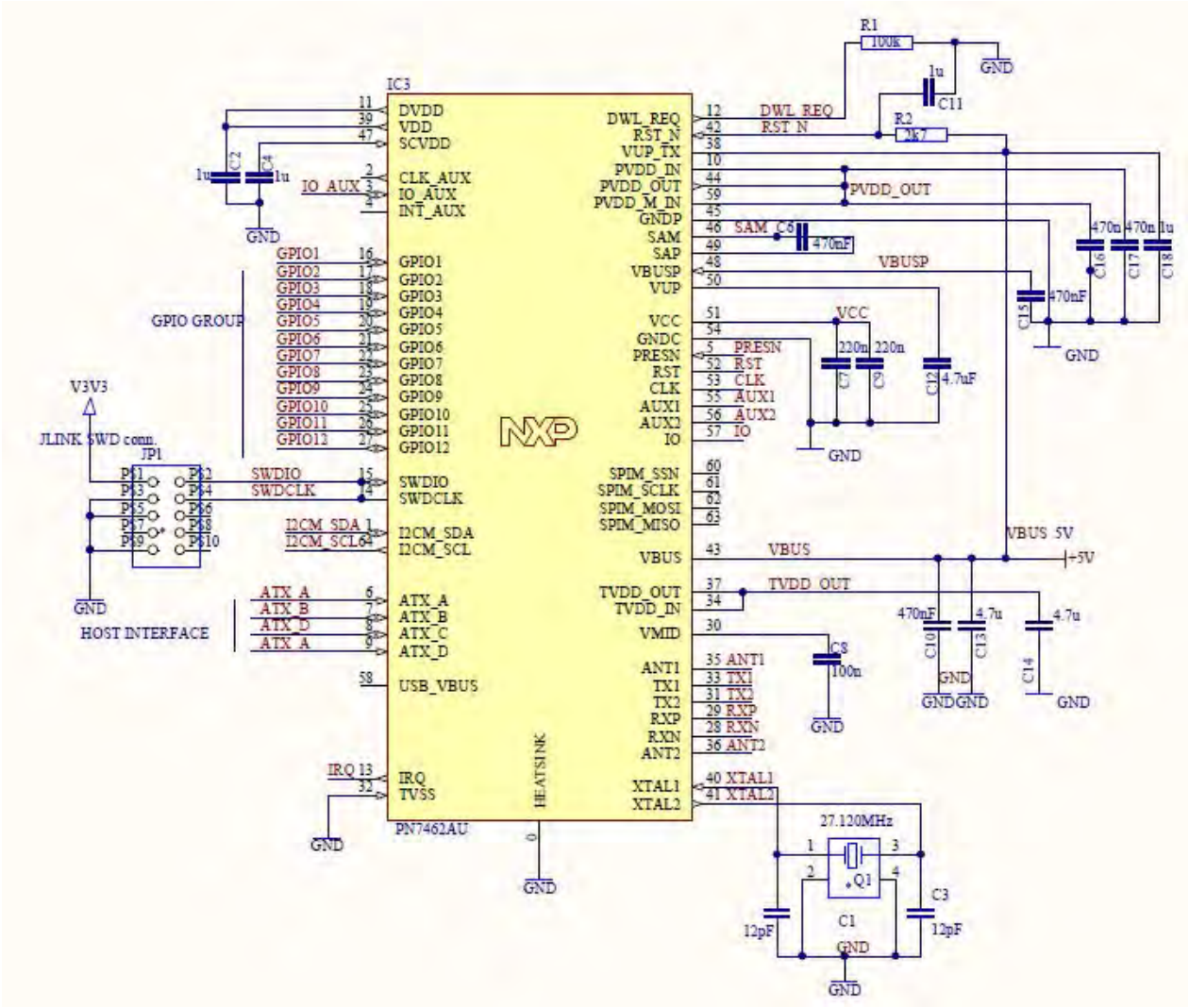
Fig 17. PN7462AU Layout Reference Board Bottom layer

4. PN7462AU hardware design

The PN7462AU is optimized to support the NFC, ISO and EMVCo with a minimum of additional components. The PN7462AU simply requires the antenna matching circuitry, some block capacitors and the crystal.

However, the calculation and tuning of the matching components need to be done carefully to provide the full performance as well as to meet CE and FCC regulations.

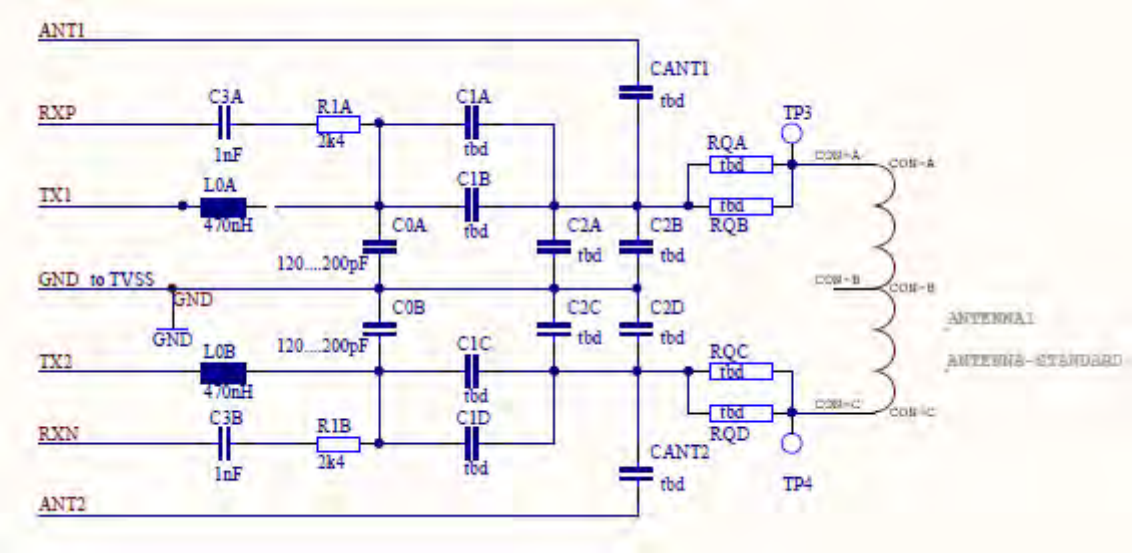
The Fig 18, Fig 19 and Fig 20 show a typical analog circuitry using the PN7462AU.



(1) Tbd: “to be defined”, need to be defined using this document.

(2) CXx, CAntx, C0x, C1x and C2x must be NP0.

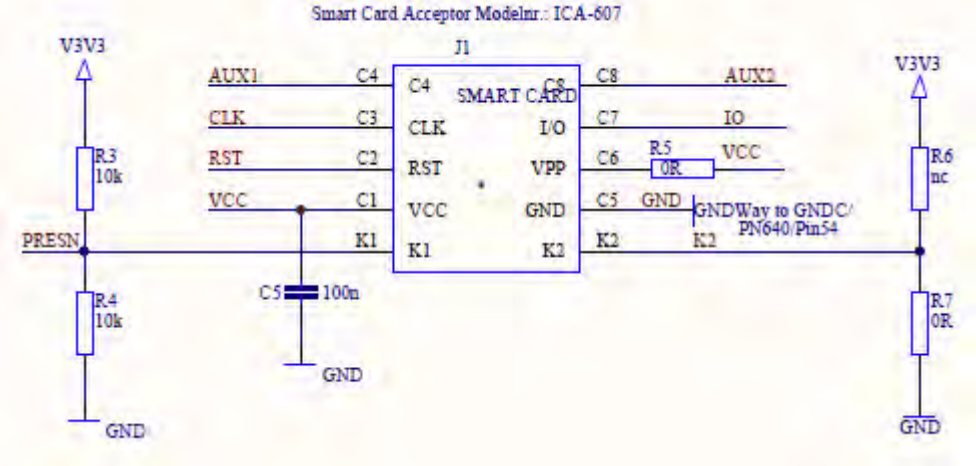
Fig 18. Typical PN7462AU analog circuit, PN7462AU part



(1) Tbd: “to be defined”, need to be defined using this document.

(2) CXx, CAntx, C0x, C1x and C2x must be NP0.

Fig 19. Typical PN7462AU analog circuit, antenna part



(1) Contact smartcard interface

Fig 20. Typical PN7462AU analog circuit, contact interface part

The antenna typically is a part of the PCB design (see section 3.2). All capacitors are typical ceramic capacitors (e.g. X7R), except the capacitors used in the matching

circuitry and those connected to the crystal. Those capacitors CXx, CAntx, C0x, C1x and C2x must be NP0.

The inductor L0x must be capable of driving the required power: In case the maximum output power is needed, the L0x must be able to drive the 200mA without going into saturation.

Note: Be aware of tolerances! The most critical tolerance in the antenna circuits appears at the antenna coil itself, but even for the matching circuitry tolerances of < ±1% are recommended.

4.1 PN7462AU requirements

The PN7462AU is optimized to support the EMVCo operating volume. Therefore the Tx output can drive up to ITVDD = 250mA. Based on a power supply voltage VBUS = TVDD = 5V that means a possible total power consumption for the total antenna circuit of up to P_{tot} > 1,25W.

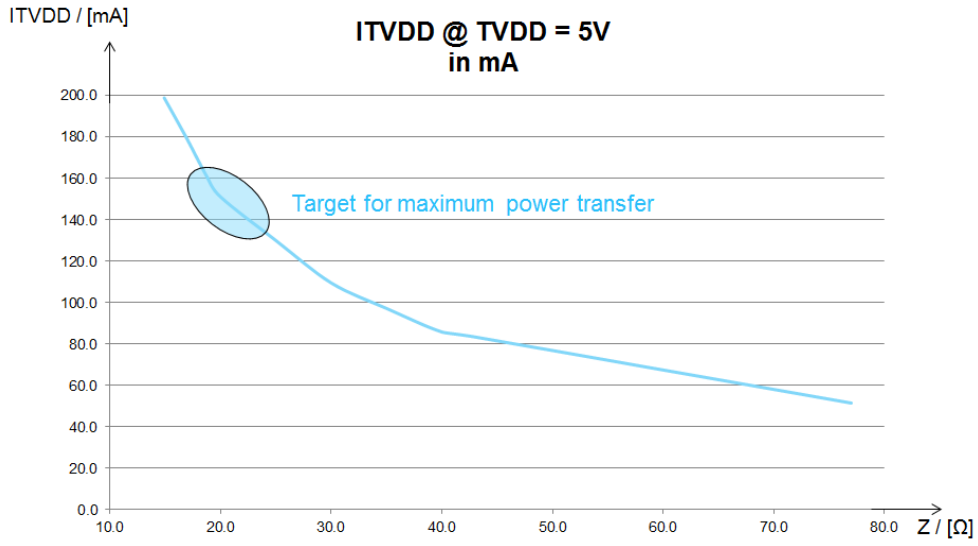
The power supply must be designed properly to be able to deliver a clean supply voltage.

Note: Every noise level on top of the supply voltage can disturb the performance of the PN7462AU. Therefore sometimes higher values of the block capacitors in the range of up to 10µF might help to improve the performance.

4.1.1 Target impedance

The PN7462AU provides an NMOS/NMOS Push-Pull output stage to drive the antenna circuit. The output impedance of each Tx outputs is approximately 1…3 Ohm (with maximum GSN settings), so basically the antenna impedance itself controls the ITVDD, and therefor the field strength.

The Fig 21 shows the driver current ITVDD versus the antenna impedance. The target impedance to get a maximum field strength and power transfer should be close to 20Ω.



(1) Antenna impedance tuned and measured between TX1 and TX2

Fig 21. ITVDD versus antenna impedance

4.2 Antenna for reader mode

If the PN7462AU is used in pure reader mode only, i.e. the PN7462AU is not used in card mode or as passive P2P target, the ANT1 and ANT2 pins do not need to be used.

In such case the CAntx are not used, and the corresponding design is done without considering the PLM (passive load modulation).

4.2.1 Antenna matching

For the proper antenna design the antenna impedance must be measured using an impedance analyzer or VNA (vector network analyzer). Such a VNA can be a high end tool from Agilent or Rohde & Schwarz (like the R&S ZVL (see [7]), as normally used in this document), but might be a cheap alternative with less accuracy like e.g. the miniVNA Pro (see [8]). In any case the analyzer needs to be able to measure the impedance in magnitude and phase (vector).

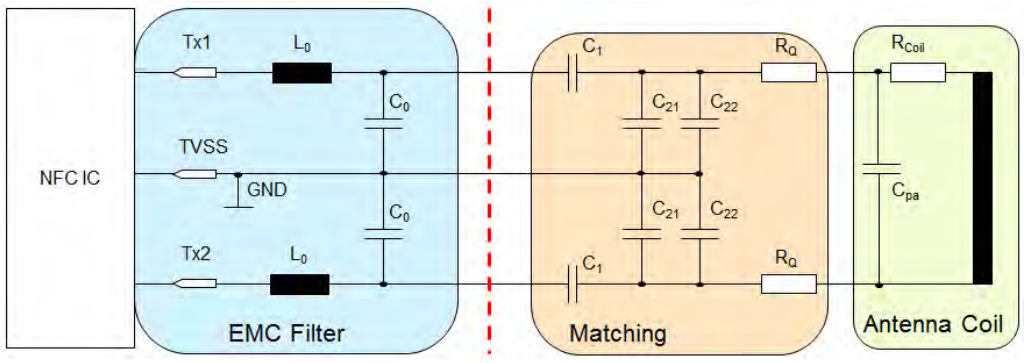
Such VNA can be used to measure the antenna coil as well as the antenna impedance including the matching circuit.

The antenna matching is done with the following steps:

1. Measure the antenna coil
2. Define target impedance and Q-factor
3. Define the EMC filter

4. Calculate the matching components
5. Simulate the matching
6. Assembly and measurement
7. Adaptation of simulation
8. Correction and assembly

The details of those steps are described in with an example, using the PN512 Bueboard antenna together with the PN7462AU. The blocks and components are used as shown in Fig 22.



(1) This circuit only covers the Tx part.

Fig 22. PN7462AU Reader only antenna matching circuit

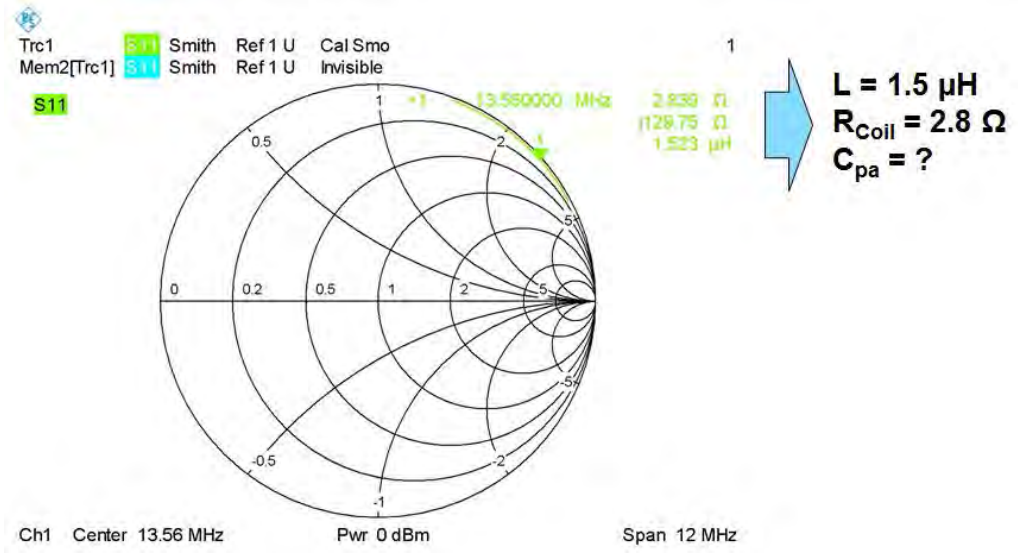
4.2.1.1 Measure the antenna coil

The antenna coil must be designed as described in section 3 and be measured. The measurement is required to derive the inductance L, the resistance R_{Coil} and the capacitance C_{pa} as accurate as possible.

The easiest even though not most accurate way is to use the VNA to measure the impedance $\underline{Z}$ of the antenna coil at 13.56MHz and to calculate L and R out of it:

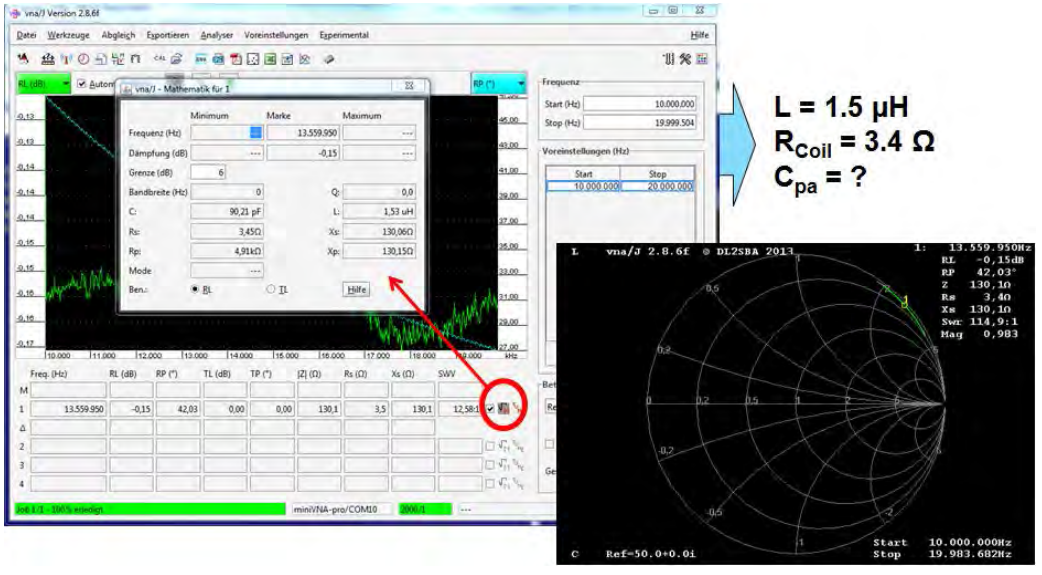
$$\underline{Z} = R + j\omega L_{Coil} \quad (4)$$

Typically the VNA directly can show the L and R, as shown in Fig 23 and Fig 24.



(1) Measurement with R&S ZVL

Fig 23. Measurement 1 Antenna coil of PN512 Blueboard



(1) Measurement with miniVNA Pro and vna/J

Fig 24. Measurement 2 Antenna coil of PN512 Blueboard

In this example the antenna coil is measured with these values:

L = 1.5 µH

R_{Coil} = 2.8 … 3.4Ω

C_{pa} = not measured, can be estimated

The inductance can be measured quite accurate, but the resistance is not very accurate due to the relationship between R and jωL. And the capacitance is not measured at all with this simple measurement.

There are several ways to improve the accuracy and even further derive the capacitance, but these simple results are enough to start the tuning procedure. This tuning procedure needs to be done anyway, so there is no real need to spend more effort in measuring the antenna coil parameters more accurate.

4.2.1.2 Define target impedance and Q-factor

The target impedance must be defined. For the maximum power transfer it should be 20Ω (as indicated in section 4.1.1). In such case the driver current ITVDD gets close to the maximum allowed limit of ITVDDmax = 200 mA.

The impedance target might be different for different applications. An impedance target of Rmatch = 50…80Ω might be better in battery powered devices, where the current consumption must be minimum, while at the same time the required maximum operating distance can be lower.

Note: The following examples show the design for a maximum power transfer, e.g. for an EMVCo POS design.

The quality factor Q depends on the overall system requirements and frame conditions. The overall system requires the Q to be in a range, which allows us to meet the timing and pulse shape requirements of the corresponding standard (ISO, NFC or EMV). These requirements are mainly the same, but with some differences:

While ISO allows data rates of up 848 kbit/s, NFC allows the data rates of up to 424 kbit/s. EMV systems are limited to 106 kbit/s. So typically the Q of EMV reader systems can be higher than the Q of ISO or NFC reader systems.

The Q is an indirect value, since the measurement of the Q in the overall antenna system, which includes the antenna driver as well as the contactless card, is complex – and not required. The wave shape and timing measurements, as required according to the standards, are the relevant measurements, and the corresponding Q value is not of any importance.

Here in a first step the Q is chosen for the passive and linear antenna circuit only. So it can be seen as start value to calculate the damping resistors R_Q.

Good starting values as entry for the calculation of the matching calculation are shown in Table 1.

Table 1. Q-factor

Values for the passive linear antenna circuit only.

Q	Condition
20	Start value for the matching calculation for typical NFC Reader design.
25	Start value for the matching calculation for typical NFC Reader design, limited to 106kbit/s.
30	Nominal value for MIFARE (Classic) communication.

Note: The lower the Q, the better the stability and robustness of the antenna is. Antennas with lower Q show less detuning. The higher the Q, the higher the field strength is.

Note: The final Q must be tuned with the pulse shape measurements, if the antenna shall be fully optimized.

Note: It might be helpful to slightly adapt the Q in the given Excelsheet calculation in such a way that the resulting damping resistor R_Q is calculated to be within an E-series of values (i.e. 2.7Ω or 3.3Ω, but not 2.845Ω). In such case the following calculation is more accurate, i.e. the calculation result gets closer to the measured result.

4.2.1.3 Define the EMC filter

The EMC filter can be a second order low pass filter as shown in Fig 18, and contains an inductor (L0) and a capacitor (C0). The cut off frequency defines the overall detuning behavior as well as the transfer function of the antenna circuit.

The inductor L0 needs to be capable to drive the full power into the antenna without going into saturation. The Q-factor of this inductor should be as high as possible.

Typically the inductance is in the range of

L0 = 330nH … 560nH

The cut off frequency typically should be far above the carrier frequency but far below the second harmonic:

F_{cutoff} = 14.5MHz … 22MHz

Based on this the following EMC filter values are chosen:

L0 = L0A = L0B = 470nH

C0 = C0A = C0B = 56pF + 68pF[1]

F_{Cutoff} = 20.9MHz

Note: This EMC filter is taken from the existing CLRC663 designs. The chosen values of the inductance, the cut off frequency and the corresponding capacitance have shown to be a reasonable trade-off between the transfer function for the transmit signal as well as for the receive signal on one hand and the filter function to suppress the higher harmonics on the other hand.

1. [1] Two capacitors are chosen, because they are already assembled on the evaluation board. A single capacitor of 120pF can be taken alternatively. The matching calculation should be done with the real value.

4.2.1.4 Calculate the matching components

The next step is to calculate the values of the matching circuit. The input for the Excelsheet as shown in Fig 25 needs to be:

“Measured” values:

La = L = 1533nH (measured antenna coil inductance)

Ca = C_{pa} = 0.1pF (estimated parallel capacitance of the antenna coil)

Ra = R_{Coil} = 3Ω (measured antenna coil resistance)

Preset values:

Q = 25 (defined Q-factor, see section 4.2.1.2)

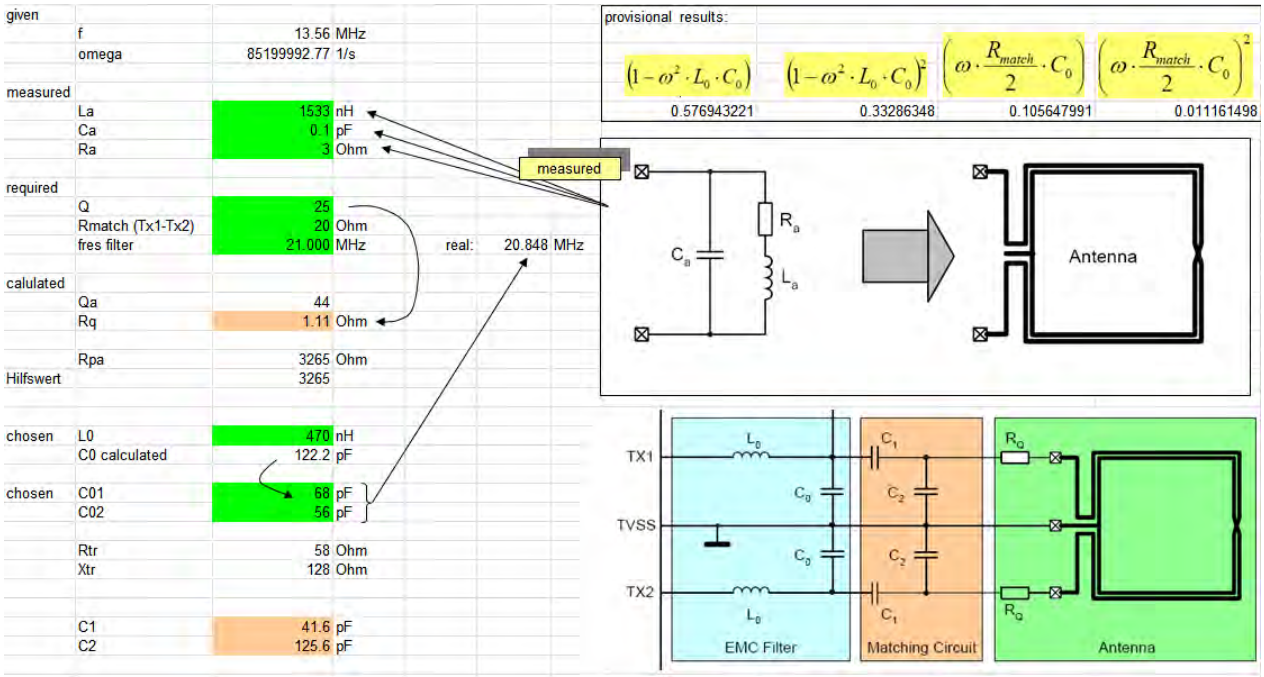
Rmatch = 20Ω (defined target impedance, see section 4.2.1.2)

L0 = L0A = L0B = 470nH (EMC filter inductance, see section 4.2.1.3)

C0 = C0A = C0B = 56pF + 68pF (EMC filter capacitance, see section 4.2.1.3)

Calculated Values (see Fig 25):

Rq = R_Q = 1.1Ω



(1) Excelsheet from www.nxp.com

Fig 25. Antenna matching calculation

The matching capacitors are calculated:

C1 = (C1A + C1B) = (C1C + C1D) = 41.6pF -> 33pF + 8.2pF (0.4pF less)

C2 = (C2A + C2B) = (C2C + C2D) = 125.6pF -> 68pF + 56pF (1.6pF less)

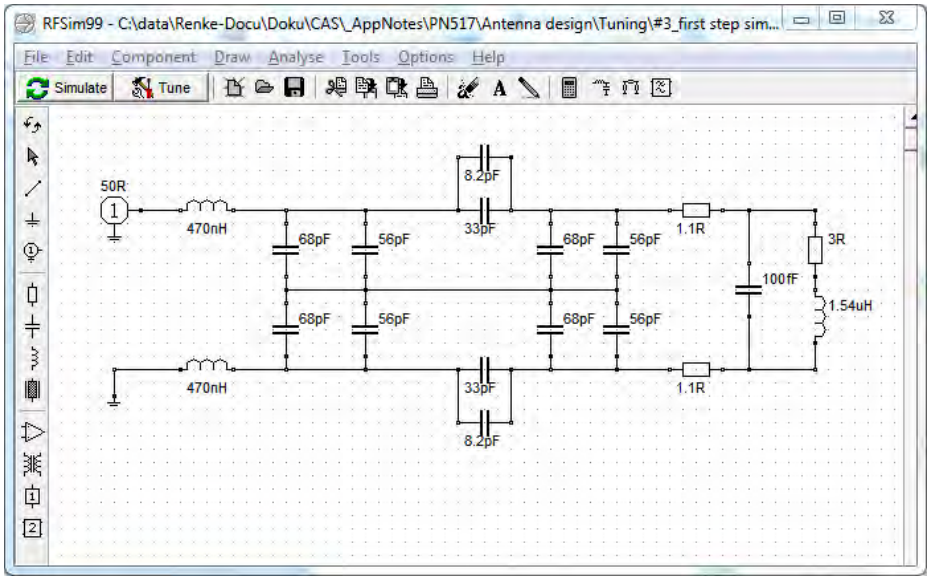
4.2.1.5 Simulate the matching

The measurement of the antenna coil itself typically is not very accurate. Therefore a (fine) tuning of the antenna normally is required, which might become easier in combination together with a simulation.

A simple matching simulation tool like e.g. RFSIM99 (refer to [10]) can be used to support the antenna tuning. The simulation input and the result based on the above given start values for the antenna matching is shown in Fig 26 and Fig 27.

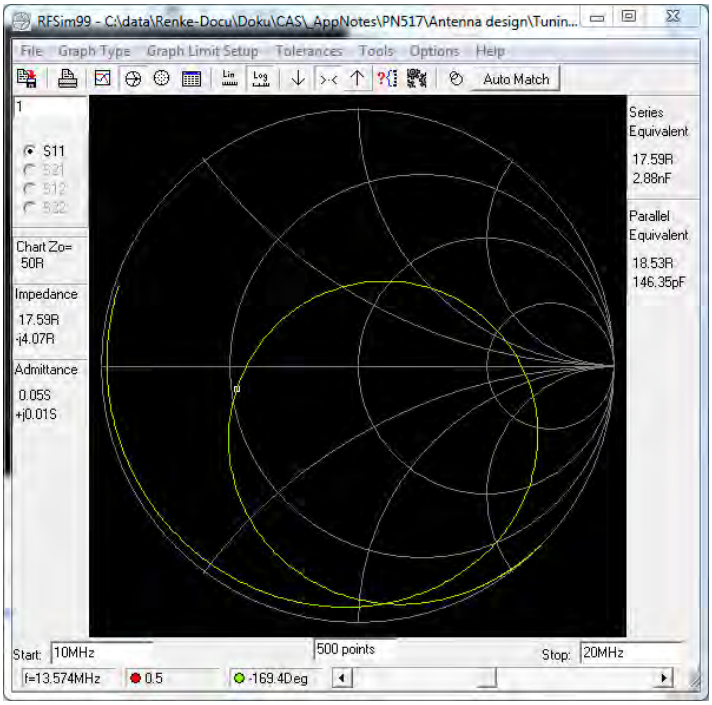
With these values the assembly can be done, even though the result is not yet optimum, as shown in Fig 27. The overall impedance is slightly below 20 Ω and capacitive (-j4Ω).

Note: The result is not as calculated, since not the exact calculated values of the capacitors are taken for assembly.



(1) The “measurement GND” is not the PN7462AU and evaluation board GND!

Fig 26. RFSIM99 Schematic

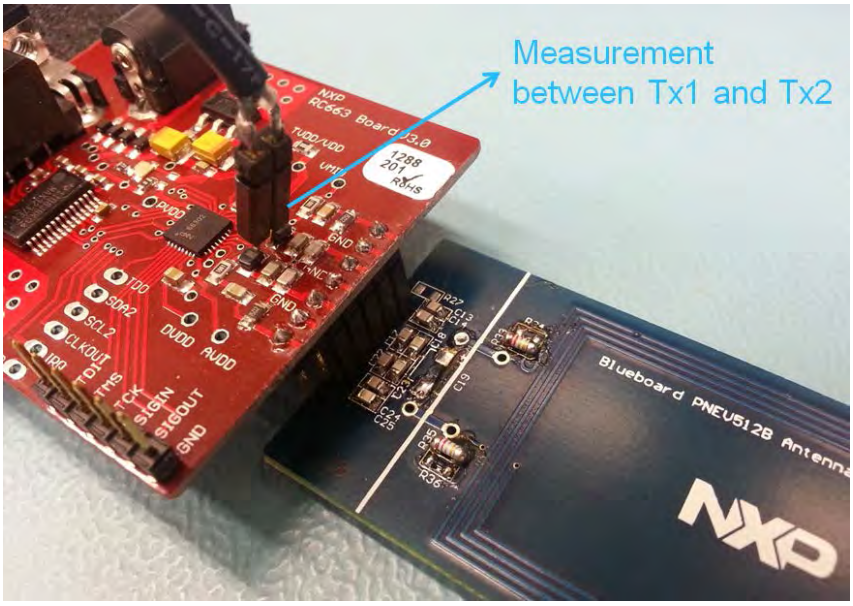


(1) Simulation based on the first calculated start values.

Fig 27. RFSIM99 Simulation result

4.2.1.6 Assembly and measurement

After the first assembly the impedance measurement must be done, as shown in an example in Fig 28.

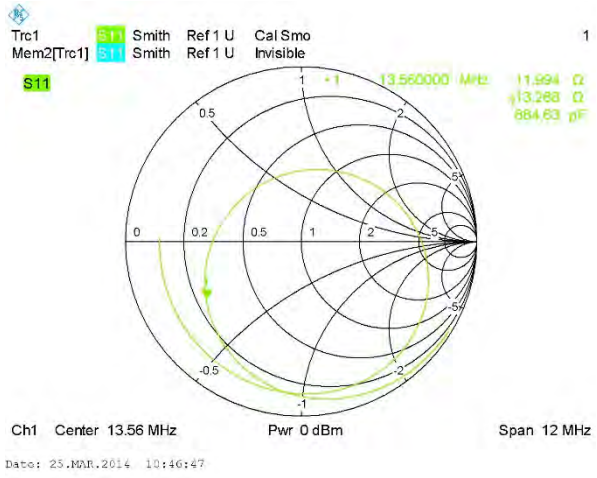


(1) A simple connector is soldered between TX1 and TX2 to simplify the impedance measurement.

Fig 28. Impedance measurement example

The measurement result is shown in Fig 29. The circuit does not meet the requiremements, i.e. it needs to be retuned.

The measurement result is typically slightly different than the simulation result, since the accuracy of the original antenna coil measurement is limited.



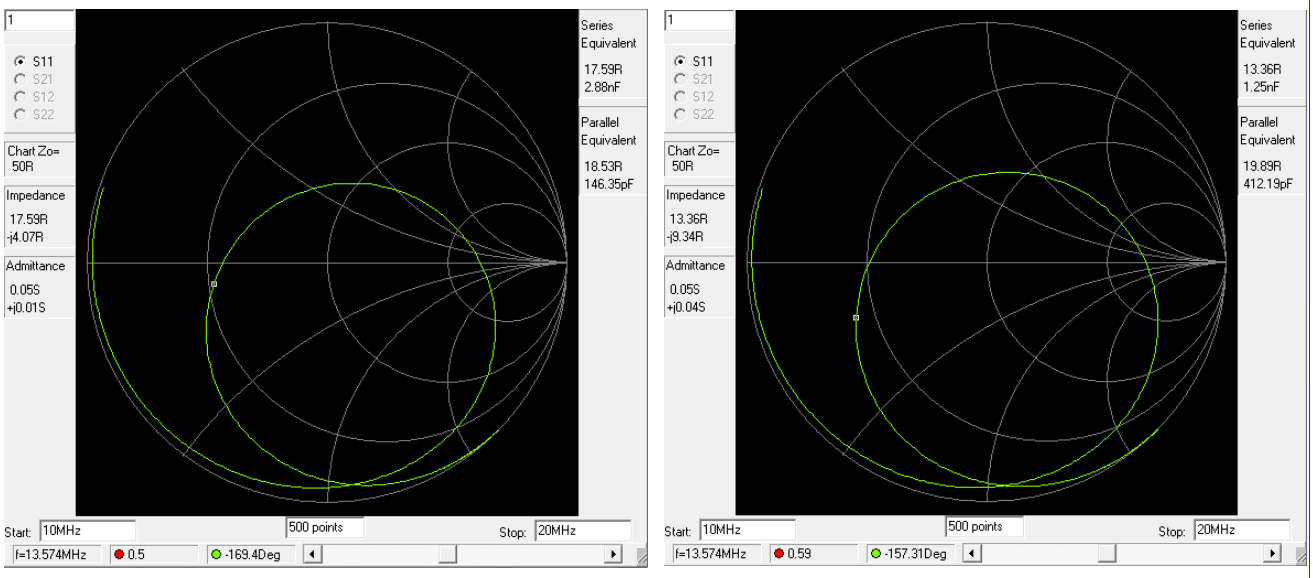
(1) This matching does not meet the requirements. It must be corrected and retuned.

Fig 29. Measurement result of first assembly

4.2.1.7 Impedance adaptation in simulation

The easiest and fastest way to (fine) tune the antenna is to first of all adapt the simulation in such a way that it shows the same result like the reality. The parameters of the antenna coil are the parameters to be changed, since these parameters are not measured (or estimated) correctly.

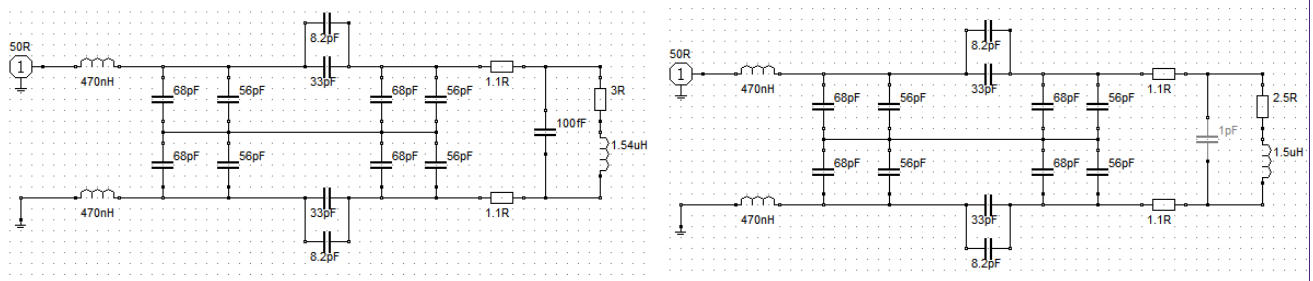
So with the values of L, C_{pa}, and R_{Coil} the simulation is tuned from Fig 29a to Fig 29b. The changed values can be seen in Fig 30b.



a. Impedance first step

b. Impedance after adaptation

Fig 30. Impedance adaptation in the simulation (result)



a. Circuit first step

b. Circuit after adaptation

Fig 31. Impedance adaptation in the simulation (circuit)

With these adapted values of the antenna coil the last step of the final tuning can be done:

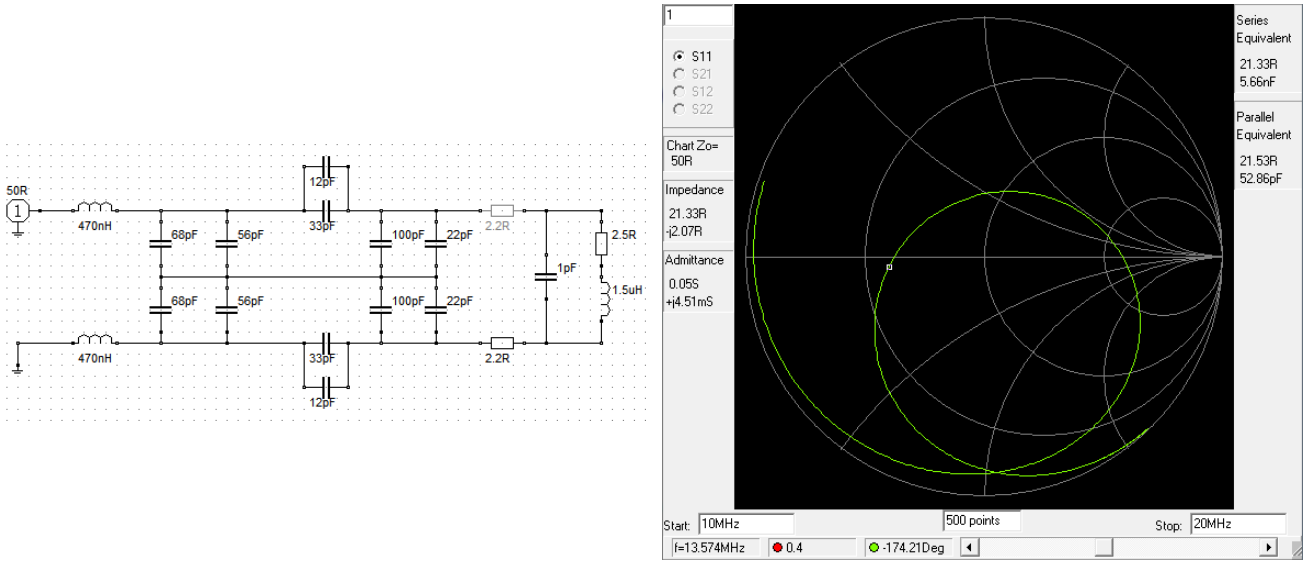
La = L = 1.5µH

Ca = C_{pa} = 1pF

$Ra = R_{Coil} = 2.5\Omega$

4.2.1.8 Impedance correction and assembly

The tuning of the impedance is now corrected with the values of C1 and C2, as shown in Fig 32.

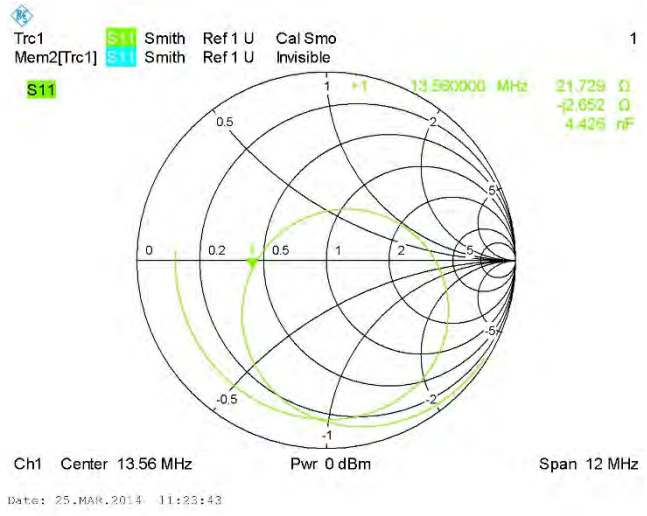


a. Final simulation circuit

b. Final Simulation result

Fig 32. Final tuning simulation

These values are assembled, and the impedance is measured. The result is shown in Fig 33.



(1) This impedance is measured unloaded.

Fig 33. Final tuning measurement result

4.2.2 Loading effect

The target impedance of the antenna design defines the ITVDD (driver current of the PN7462AU) and the output power (i.e. operating distance for a given antenna coil) as shown in section 3.

The lower the impedance gets, the higher the ITVDD becomes. Especially for high power reader design, where the impedance is quite low to achieve a maximum of field strength (as e.g. shown in Fig 7), the ITVDD might get close to its limit. In worst case loading conditions the ITVDD might even exceed the specification limits and therefor reduce the life time of the PN7462AU.

So in any case it is strongly recommended to check the loading and detuning of the antenna.

The first step is to check two typical and extreme use cases:

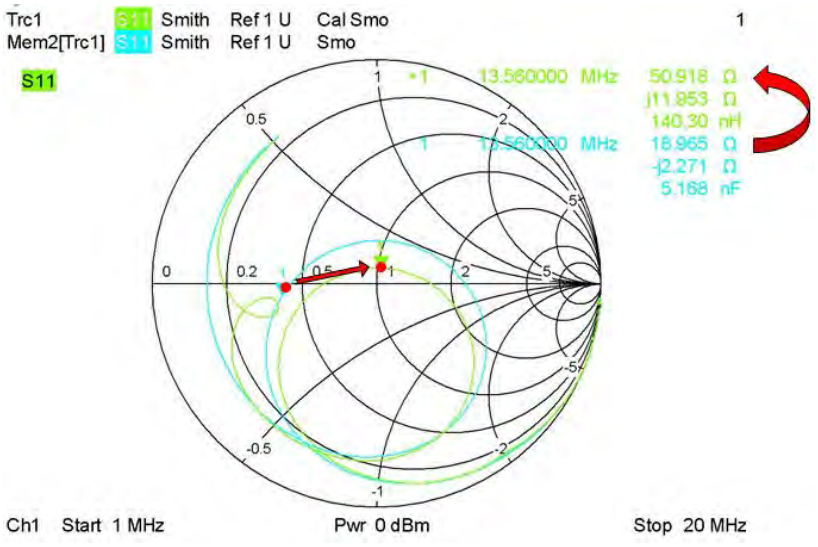
1. Loading with Reference PICCs
2. Loading with a metal plate

Both cases must be tested under real operating conditions to ensure the ITVDD limit (“active” loading, see 4.2.2.3), but it is very helpful to check the “passive” loading and understand its behavior.

4.2.2.1 “Passive” loading with ReferencePICCs

The loading with ReferencePICCs being calibrated for the Hmin test show a kind of worst case loading with typical PICCs, since this is the purpose of calibrated Reference PICCs.

The Fig 34 shows the unloaded impedance curve (blue) as well as the loaded curve (green), when the antenna is loaded with a ReferencePICC. In this case the Reference PICC is place closely to the antenna to achieve the maximum possible coupling between PCD and PICC.



(1) ITVDDloaded < ITVDDunloaded

Fig 34. Antenna impedance example with Reference PICC loading

The change of the impedance curve indicates a lower ITVDD under loading conditions. That implies that with the above shown antenna matching the loading with ReferencePICCs (or typical smart cards) does even decrease the field strength and ITVDD. This even sometimes helps to meet the maximum EMVCo limits for power transfer, especially with small antennas.

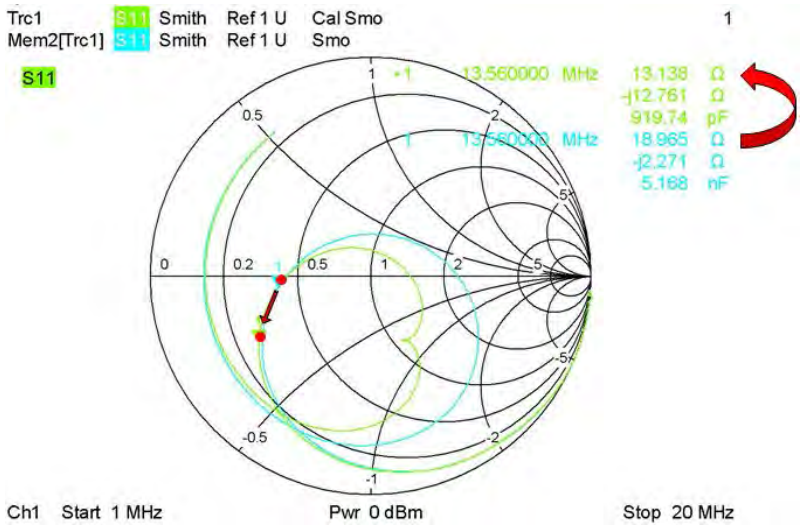
This loading must be cross checked under normal operating conditions (see 4.2.2.3).

Note: The loading with the ReferencePICC typically turns the impedance circle in the smith chart clockwise. At the same time the overall Q-factor drops, so the circle gets smaller. Due to the tuning of the antenna, the impedance almost stays resistive, but moves towards a higher impedance. A new resonance (small loop) at a frequency above 13.56MHz can be seen: this is related to the resonance frequency of the ReferencePICC itself.

4.2.2.2 "Passive" loading with metal

The other most critical case typically is the loading with some large metal plate. Such metal plate e.g. might even be an NFC tablet or a large NFC phone.

The Fig 35 shows the unloaded impedance curve (blue) as well as the impedance curve, when a large smart phone loads the antenna (green), where the battery acts as a magnetic short cut. In this example the worst case loading effect occurs in almost 2cm distance.



(1) ITVDDloaded > ITVDDunloaded

Fig 35. Antenna impedance example with smart phone loading

As can be see, in this case of metal loading the ITVDD must increase, since the overall impedance gets lower:

$$Z_{unloaded} = \underline{|Z|} \approx 19\Omega$$

$$Z_{loaded} = \underline{|Z|} \approx \sqrt{13.14^2 + 12.76^2} = 18.3\Omega$$

This behavior needs to be checked carefully, directly measuring the ITVDD.

4.2.2.3 “Active” loading

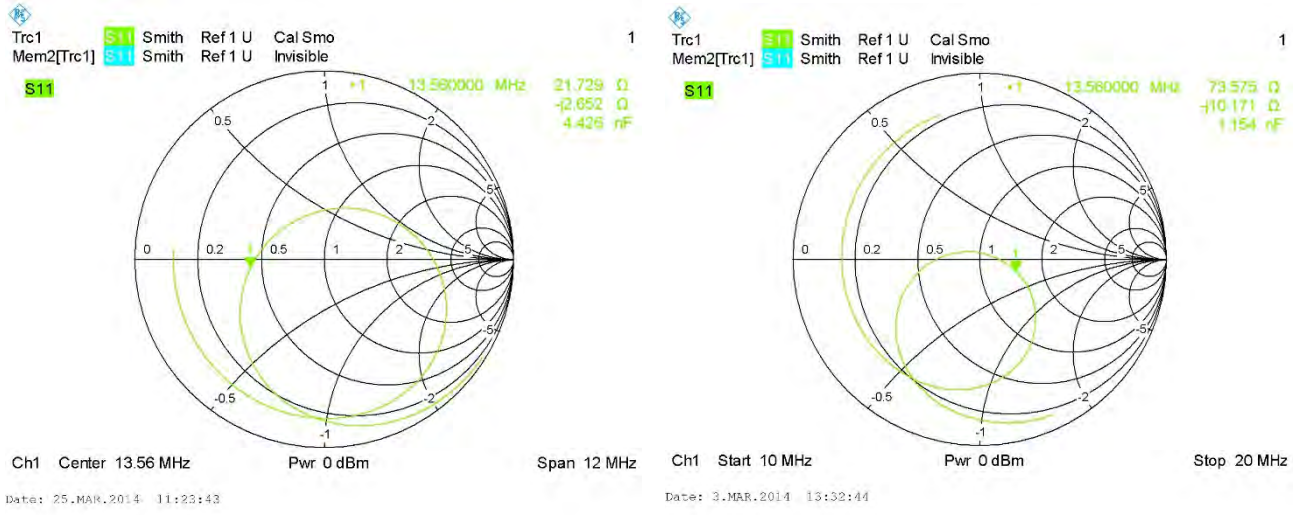
The impedance measurement as shown above is always done with limited power (typically 0dBm), so especially the ReferencePICC shows a slightly different behavior than in the real test case. Therefore the “passive” loading measurement can only show the trend of loading and detuning, but does not allow a 1:1 calculation of the related ITVDD out of the impedance.

So finally the loading must be tested under real operating conditions, i.e. the PN7462AU must be powered and the carrier must be enabled. Then the ITVDD must be measured under the different loading conditions (see above). In no case the ITVDD is allowed to exceed the specification limit.

4.3 Antenna for all NFC modes

The antenna design to support all NFC modes is done in the same way as described in section 4.2, except the PLM connection, using the CANT1 and CANT2. The two related pins of the PN7462AU (ANT1 and ANT2) are used to drive the passive load modulation (PLM) in card emulation mode or when the PN7462AU is used as passive target.

Typically the NFC antenna design uses higher target impedances even in reader mode (RM), since the required operating volume is much smaller and at the same time the current consumption must be as low as possible. For impedances higher than 50Ω it might be better to target a “parallel” resonance as shown in Fig 36b.



a. “Serial” resonance (low impedance)

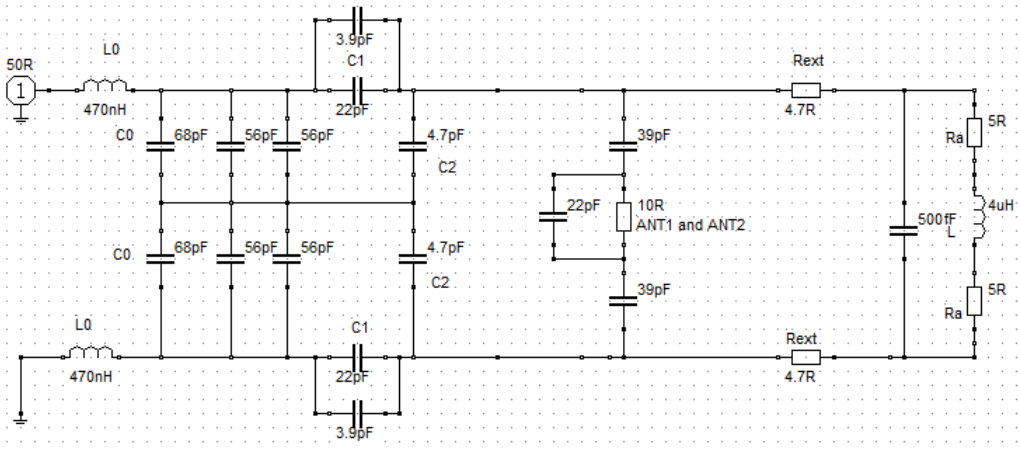
b. “Parallel “ resonance (high impedance)

Fig 36. RM Antenna matching with low and high impedance

4.3.1 Antenna tuning for RM and CM

The antenna tuning supporting both reader mode (RM) and card mode (CM) needs to consider the ANT1 and ANT2 pins of the PN7462AU. In CM these pins are in “high Z” state, in RM the ANBT1 and ANT2 are low.

The Fig 37 shows the simulation of the NFC antenna in RM. The ANT1 / ANT2 connection is simulated and measured with a 10Ω resistor.

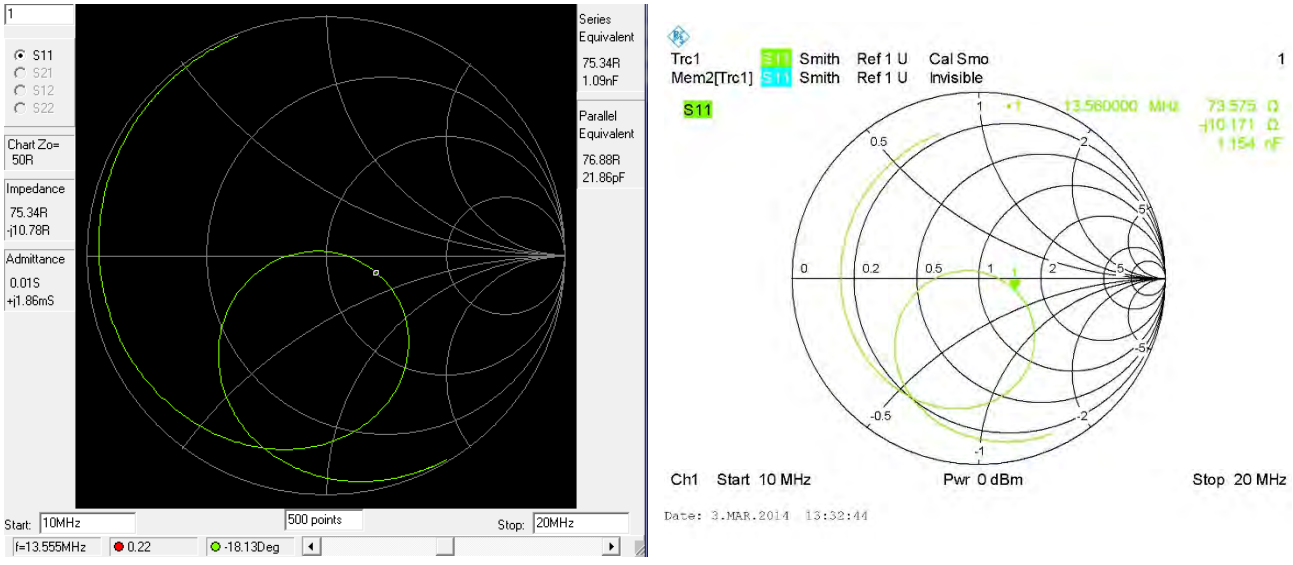


(1) 10Ω||22pF for simulation of the PN7462AU (ANT1 and ANT2) in RM

Fig 37. NFC antenna in RM

The Fig 38 shows the simulation and measurement result.

Note: The measurement must be done with 10 bridging the ANT1 and ANT2 pins.

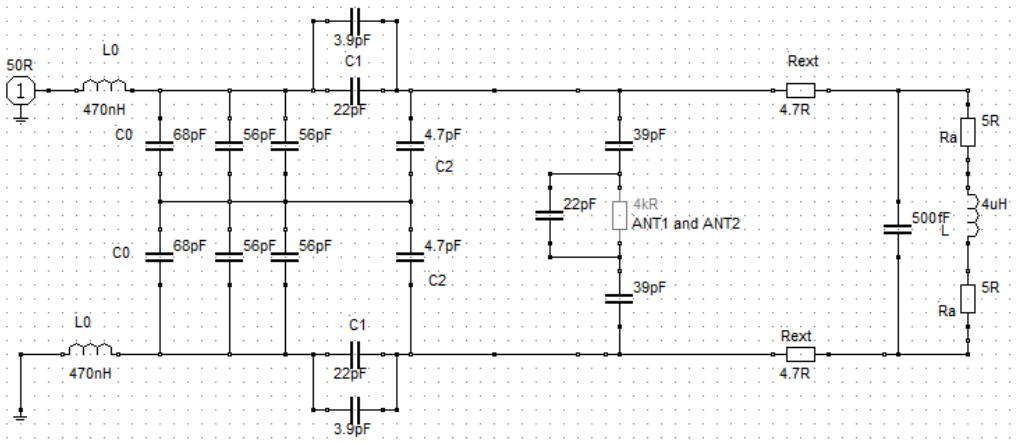


a. Simulation

b. Measurement

Fig 38. Impedance of the NFC antenna in RM

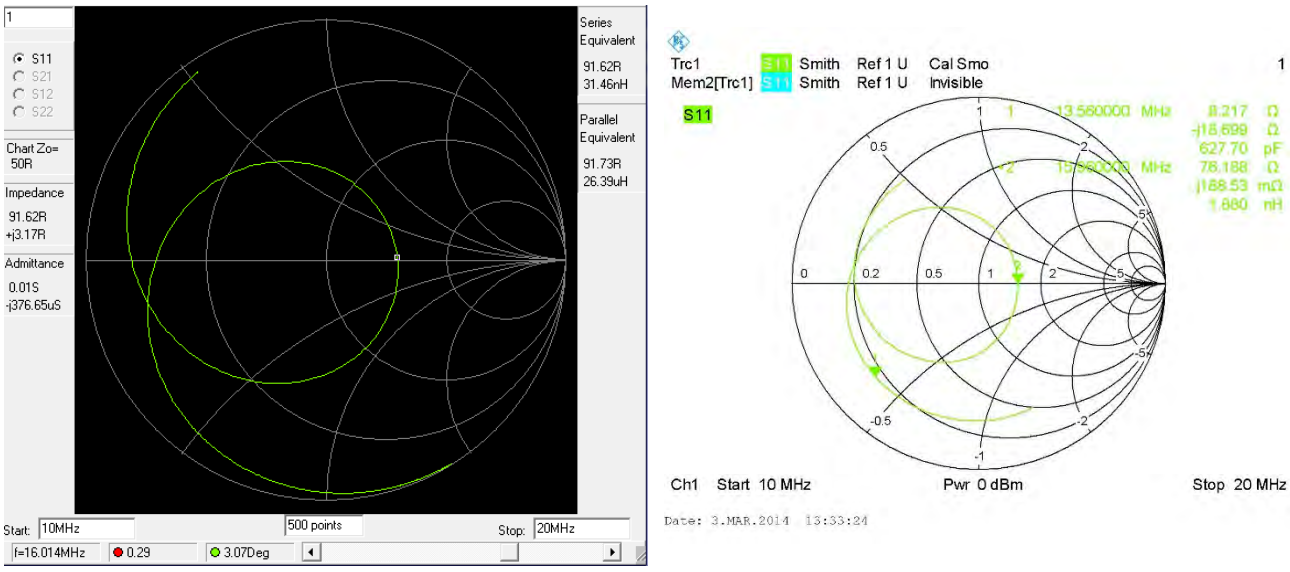
In CM the ANT1 and ANT2 pins are floating (“high Z”), which can be simulated with approximately 4kΩ || 22pF, as shown in Fig 39.



(1) 4kΩ||22pF for simulation of the PN7462AU (ANT1 and ANT2) in CM

Fig 39. NFC antenna in CM

The simulation and measurement result is shown in Fig 40. The resonance frequency in CM is approximately 16MHz.



a. Simulation

b. Measurement

Fig 40. Impedance of NFC antenna in CM

4.4 Optimizing the transmitting

In a typical PCD design the output stage of the PN7462AU is used with the maximum available output power, and the overall power consumption (and field distribution) is limited with the antenna impedance.

The standard modulation of the Tx signal is either a 100% AM for type A or a 10% AM for type B. The modulation index for type B must be adjusted due to the antenna tuning with the CLIF_ANA_TX_AMPLITUDE_REG.

On top it might be helpful to adapt the rise and fall times of the Tx envelop signal to match the pulse shapes to the timing requirements of the according standard (NFC, ISO or EMVCo).

The optimum register settings might be different from the default values stored in the EEPROM. So for the optimization and testing typically the registers can be tuned and changed directly. As soon as the optimum settings are derived, the new settings might be changed and stored in the corresponding EEPROM area for the LOADPROTOCOL. Then in the final application simply the standard LOAD_PROTOCOL command can be used again with the optimized settings, and no modification of the application sw is required.

The default settings in the EEPROM are optimized for the PN7462AU based on the evaluation board antenna. Some of these settings might be adjusted and optimized for other antenna designs.

The major parameters for the Tx are:

1. Modulation pulse width (normally not required to be changed)
2. Modulation index (for type B)
3. TX_Clockmode (for type A, if needed)
4. Tx Shaping (rise and fall time, if needed)

4.4.1 Modulation pulse width

The modulation pulse width is adjusted with the TX_S23_MODWIDTH (CLIF_TX_SYMBOL23_MOD_REG) and TX_DATA_MOD_WIDTH (CLIF_TX_DATA_MOD_REG). Both values must be the same, and are typically automatically set with the LOADPROTOCOL. Normally no optimization is needed.

4.4.2 Type B Modulation index

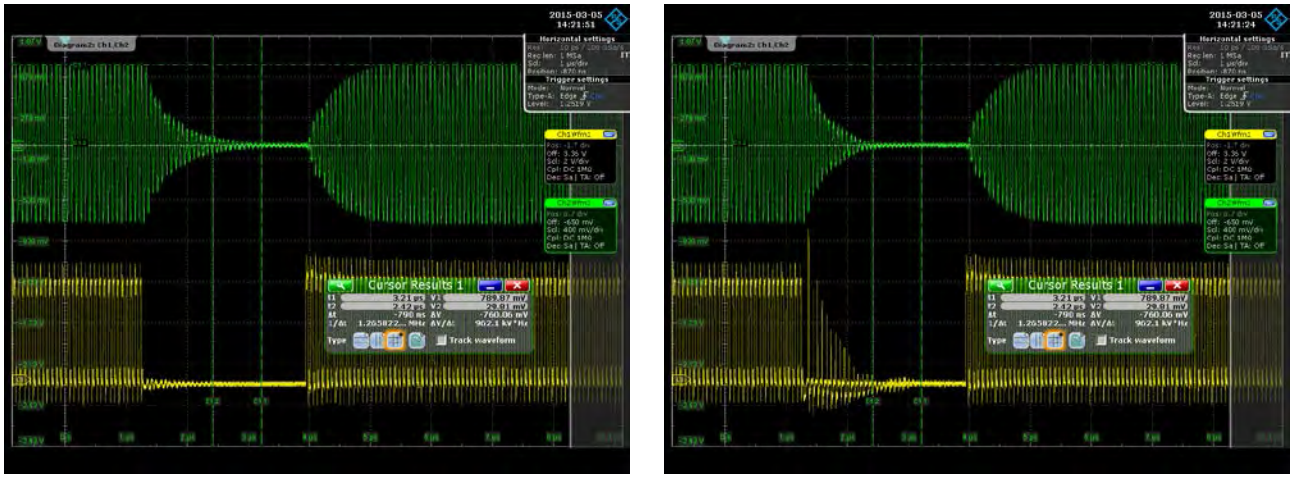
For type B the modulation index needs to be checked and maybe adjusted, since the final optimum setting depends on the antenna design. The LOADPROTOCOL provides the correct settings, which are required for type B, but the modulation index must be set with TX_RESIDUAL_CARRIER (CLIF_ANA_TX_AMPLITUDE_REG), as described in detail in [1].

4.4.3 Tx envelope shape

The PN7462AU provides some registers to adjust the wave shapes. The following description is based on the default settings from the LOADPROTOCOL of the corresponding protocol (type A or type B).

4.4.3.1 TX_CLK_MODE

For type A the 100% ASK is enabled, so basically no residual carrier needs to be adjusted. However, the TX_CLK_MODE_RM (CLIF_ANA_TX_CLK_CONTROL_REG) allows to change the TX output stage behavior during the modulation pulses. The Fig 41 showsan example with the default setting as well as the setting, where the TX output stages are open drain, and only the low side MOS (pull) are actively driven. The green signal shows the field, picked up with the ReferencePICC in a few cm distance. The yellow signal shows the TX output using a standard probe with a standard GND cable. These signals just indicate the difference between different register settings in principle.



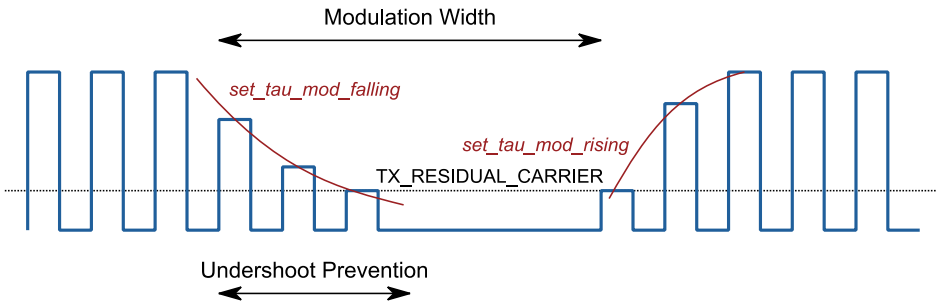
a. TX_CLK_MODE_RM = 001bin (Default)

b. TX_CLK_MODE_RM = 101bin (low side pull)

Fig 41. TX_CLK_MODE_RM

4.4.3.2 TX_SHAPE_CONTROL

The CLIF_ANA_TX_SHAPE_CONTROL_REG allows to adjust the shape of the falling and rising edges of the Tx envelope signal (see the principle in Fig 42).



(1) TX_SET_TAU_MOD_FALLING & TX_SET_TAU_MOD_RISING

(2) TX_SET_SLEW_SHUNTREG

Fig 42. Tx envelope shaping

The fastest rise and fall times (only defined by the system-Q factor) – exemplarily shown in Fig 41 (right hand side) - can be achieved by means of using:

No undershoot prevention (type A default setting)

TX_CLK_MODE_RM (CLIF_ANA_TX_CLK_CONTROL_REG) = 0x5 (low side pull)

The Fig 43 shows an example of a pulse shape with and without using the Tx shaping control. The figure on the left hand side uses the default settings for type A, the figure on the right hand side uses the following changes:

TX_RESIDUAL_CARRIER_OV_ PREV (CLIF_ANA_TX_SHAPE_CONTROL_REG) = 0x1D (m ≈ 50%)

TX_SET_TAU_MOD_RISING (CLIF_ANA_TX_SHAPE_CONTROL_REG) = 0x2

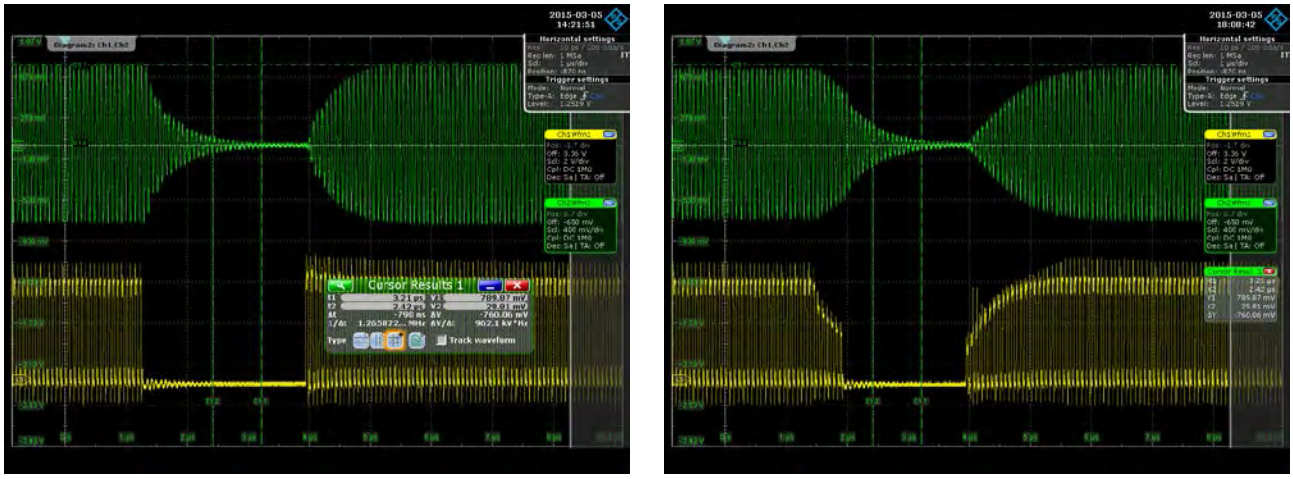
TX_SET_TAU_MOD_FALLING (CLIF_ANA_TX_SHAPE_CONTROL_REG) = 0x2

TX_SET_SLEW_SHUNTREG (CLIF_ANA_TX_SHAPE_CONTROL_REG) = 0xF

TX_UNDERSHOOT_PROT_ENABLE (CLIF_ TX_UNDERSHOOT_CONFIG_REG) = 0x1

TX_UNDERSHOOT_PATTERN_LEN (CLIF_ TX_UNDERSHOOT_CONFIG_REG) = 0x8

This shaping slows down the rising and / or falling time of the envelope and might help to meet the standard requirement, if the antenna has a very low Q.



a. No extra shaping
b. Green: Field probe
c. Tx1 signal
d. TX shaping (falling and rising edge)
e. Green: Field probe
f. Tx1 signal

Fig 43. Example of TX shaping (100% ASK envelope)

4.5 Optimizing the receiving

The Fig 44 shows the high level principle of the Rx blocks for one Rx path. The major register for the Rx are the registers related to the AGC setting,

Rx_Gain, (CLIF_ANA_RX_REG)

High Pass Corner Frequency (HPCF) (CLIF_ANA_RX_REG), and

RxThresholds (MINLEVEL and MINLEVELP)(CLIF_SIGPRO_RM_CONFIG1_REG).

The AGC is normally set to be used in automatic mode. The AGC_VALUE (which adjusts the “internal resistor”) can be read from the CLIF_ AGC_VALUE_REG.

The RxGain adjusts the analog gain of the demodulated subcarrier in the I and Q channel. The HPCF limits the bandwidth of the (modulated) sub carrier signal.

For the optimization of the Rx circuit it is recommended to use the debug and test signals as described below and in [1].

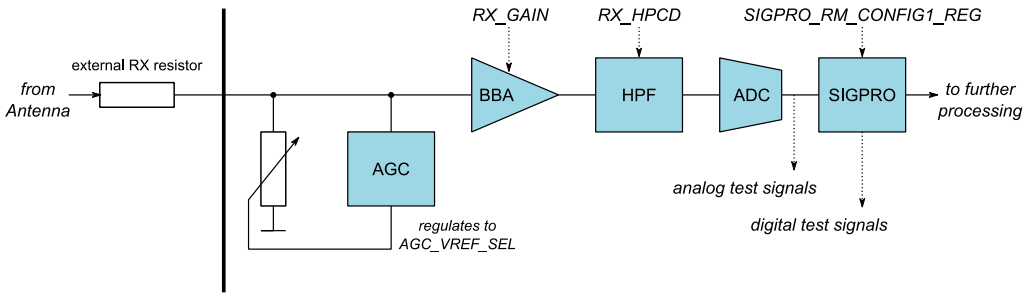


Fig 44. PN7462AU Rx block diagram

The optimum register settings might be different from the default values stored in the EEPROM. So for the optimization and testing typically the registers can be tuned and changed directly. As soon as the optimum settings are derived, the new settings might be changed and stored in the corresponding EEPROM area for the LOADPROTOCOL. Then in the final application simply the standard LOAD_PROTOCOL command can be used again with the optimized settings, and no modification of the application sw is required.

The default settings in the EEPROM are optimized for the PN7462AU based on the evaluation board antenna. Some of these settings might be adjusted and optimized for other antenna designs.

4.5.1 External Rx components

The RxP and RxN are connected to the antenna circuit. Typically there is a standard coupling capacitor used to connect the Rx circuit to the EMC filter (see Fig 18). External filtering normally is not required.

The voltage level at the RxN and RxP must be high enough to achieve a good sensitivity, but must not exceed the given limit (see [1]).

Typically the serial resistor R1A and R1B is in the range of 1…10kΩ. The exact value can be chosen with the help of the AGC. The automatic gain control (AGC) of the PN7462AU automatically adjusts the voltage level at the RxN and RxP as long as the control range is not exceeded. So a good value of R1A and R1B provides an AGC_VALUE of approximately 0x100. The test can be done in the following steps:

1. Choose R1A and R1B (e.g. start with 4.7kΩ).
2. Apply the default AGC settings (automatic operation), e.g. with the default LOADPROTOCOL for type A@106, and switch on the carrier.
3. Read the AGC_VALUE.
4. If AGC_VALUE > 0x200, then decrease R1A and R1B.
5. If AGC_VALUE < 0x080, then increase R1A and R1B.

Note: The AGC only measures the Rx voltage level of the RxP. Normally the voltage level at RxN and RxP should be the same. However, in case of wrong assembly or a bad symmetry the voltage level might be different at both pins. Therefore a voltage measurement might be useful to ensure symmetry.

Note: The voltage measurement at the RxP and RxN pins must be done with low capacitance probe (active probe) with an input capacitance of < 3pF.

4.5.2 Fix AGC

While the PN7462AU offers an automatic gain control (AGC) for the receiver voltage, it might improve the receiver sensitivity in RM, if the AGC is locked to a fix value.

When using the fix AGC, the AGC_VALUE must be set correctly in combination with the correct R1 values.

Note: When fixing the AGC it might make sense to read the AGC_VALUE upfront (with automatic AGC) to calibrate temperature drift or tolerances. In such a case the AGC_VALUE can be read using the automatic AGC, and then this value can be used and set as fix AGC_VALUE, to disable the automatic AGC.

Table 2. AGC settings example

PN7462AU Evaluation board with R1A = 5k6Ω (RXP) and R1B = 6k8Ω (RXN)

AGC_VALUE [hex]	RxN [pp]	RxN [peak]	RxN [mean]	RxP [pp]	RxP [peak]	RxP [mean]	Comment
000	2,37V	2,16V	0,97V	2,26V	2,10V	0,94V	Maximum voltage (too high)
3FF	0,24V	1,00V	0,88V	0,11V	0,94V	0,88V	Minimum voltage (too low)
0FA	1,24V	1,50V	0,88V	1,16V	1,47V	0,88V	Automatic setting (optimum)

Note: The relevant value is the peak value, which shall be as large as possible without exceeding the specified limit (refer to [1]). Typically a value of V_{Rxpeak} = 1.5V is optimum.

Note: Consider antenna loading and detuning effects!

4.6 Test and debugging

Typically the Rx does not require any specific optimization. However, in some critical cases it might help to check the register settings. In any case it is very useful to ensure the correct signal to noise level. In some cases it might be required to reduce the external noise level.

Note: To optimize the registers shown and described in the following chapter refer to Annex 5.2. In this part the tool chain is described that is used for the register optimization.

4.6.1 Digital test signals

4.6.1.1 Declaration:

```
/* GPIO4 = tx_active.
 * GPIO5 = rx_active. */
uint8_t aTestBus1Config[] = { 0x02,
    PH_EXRF_TESTBUS1_SELECT };
uint8_t aTestBus2Config[] = { 0x06,
    PH_EXRF_TESTBUS2_SELECT };
```

Red marked 2 bytes for digital test signal at GPIO4.

Green marked 2 bytes for digital test signal at GPIO5

This example declaration is routing tx_active to GPIO4 and rx_active to GPIO5

Table 3. Digital test signals

User parameter for the Api (Signal number)	Signal Name	Group TB0 ==> CLIF1 (TESTBUS1 always) GPIO4	Group TB1 ==> CLIF2 (TESTBUS2 always) GPIO5
2	TX_ACTIVE	2	2
3	TX_ENABLE	3	3
4	TX_ENVELOPE	4	4
5	RX_ENABLE	5	5
6	RX_ACTIVE	6	6

4.6.1.2 Activate digital test signal

The following System service routine is used to enable the digital test bus on GPIO4 / 5. Only these pins can be used for digital test purpose. The test signals can be activated and set separately from each other so in case only one digital test pin is used, the system service routine only needs to be called once. In case both GPIO's are needed, the routine needs to be called two times (as shown below).

```
status = phhalSysSer_CLIF_Config_DigitalTestBus((void *)
aTestBus1Config);

status = phhalSysSer_CLIF_Config_DigitalTestBus((void *)
aTestBus2Config);
```

4.6.2 Analog test signals

4.6.2.1 Declaration:

```
uint32_t dwClifAnalogTestBus[] = { 0xDD, 0x00301};
```

Red marked 2 bytes for analog test signal at GPIO2.

Green marked 2 bytes for analog test signal at GPIO1

This example declaration is routing ADC_QS to GPIO2 and ADC_Q to GPIO1.

Following test signals can be propagated to GPIO 1 and 2. The value is the full value for the second variable of the `dwClifAnalogTestBus`. The value is always shown with the same signal at both GPIO's. As shown in the example declaration it is possible to route different analog test signals to those pins.

The following table shows the possible test signals for GPIO1 as well as GPIO2

Table 4. Analog test signals

value	GPIO1 signal	GPIO2 signal
0x00101	ADC_Q	ADC_Q
0x00202	ADC_I	ADC_I
0x00303	ADC_QS	ADC_QS
0x00404	ADC_IS	ADC_IS
0x00909	BPSK_SUM	BPSK_SUM
0x00A0A	DPRESENT_SUM	DPRESENT_SUM

The Q and I signal are gripped from the analog part previous to the filter stage. QS and IS are picked up after the filter.

bpsk_sum

This test signal shows the sum of the bpsk phase jumps. Each peak of this signal indicates a detected phase jump of the activated receiver.

dpresent_sum

This signal shows the correlation of the sampled ADC signal with the subcarrier, so a high value is shown as long as the subcarrier is detected.

4.6.2.2 Activate analog test signals

The following System service routine is used to enable the analog test bus on GPIO1 / 2. Only these pins can be used for analog test purpose.

```
/* Enable the Analog Test Bus. */

status = phhalSysSer_CLIF_Config_AnalogTestBus(&dwClifAnalogTestBus[0]);
```

4.6.2.3 Example Type B

The following figures show the relevant test signals under some standard test conditions.

The Fig 45 shows a standard type B response from a ReferencePICC. The left part starts with a falling edge of the trigger signal (blue) derived from the digital test signal using the TX_ACTIVE.

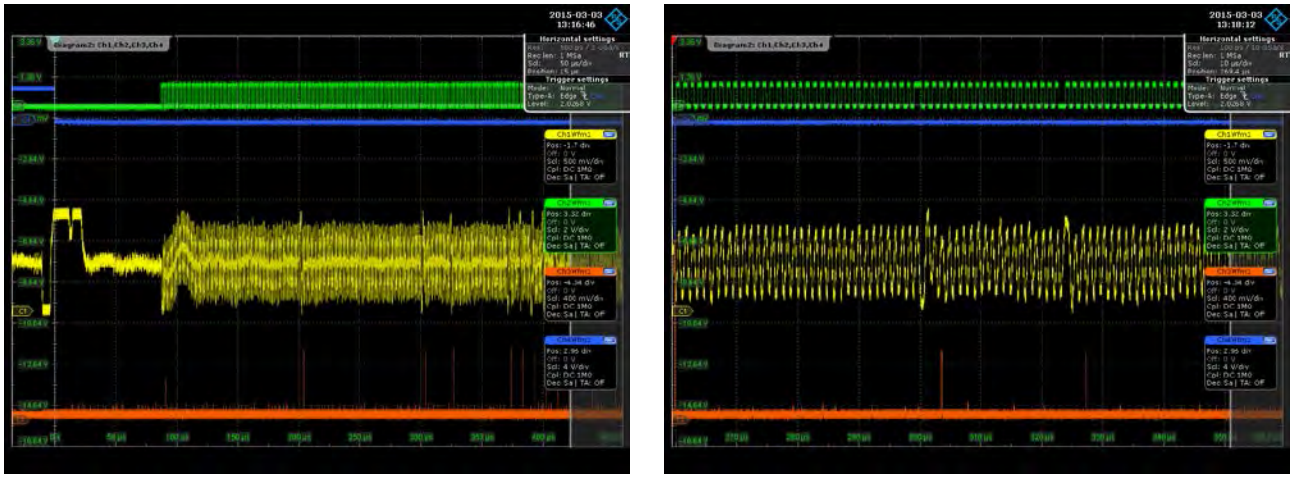
The green signal shows the LMA input at the ReferencePICC. In the center of the screenshot the first phase shift of the start of frame (SOF) can be seen.

The yellow signal shows the ADC output of the demodulated subcarrier (unfiltered Q channel).

The orange signal shows the phase shifts, as detected by the PN7462AU.

The screenshot on the right hand side of Fig 45 shows the same response with the same test signals, but horizontally zoomed in on a character of the type B response. Not only the phase shifts can be seen, but also the phase noise (noise floor in the orange signal). Depending on LMA level, coupling and noise from the PCD environment, this noise might be higher than shown in Fig 45, and then might impact the Rx performance.

Note: All the data related to the shown signals in the Fig 45, Fig 46 and Fig 47 can be received properly.



a. Type B response
b. Green: LMA (RefPICC input)
c. Blue: TX_ACTIVE (Trigger)
d. Yellow: unfiltered Q-Channel
e. Orange: BPSK_SUM
f. Type B response Zoom in
g. Green: LMA (RefPICC input)
h. Blue: TX_ACTIVE (Trigger)
i. Yellow: unfiltered Q-Channel
j. Orange: BPSK_SUM

Fig 45. Type B response with test signals

The major registers which need to be adjusted properly are:

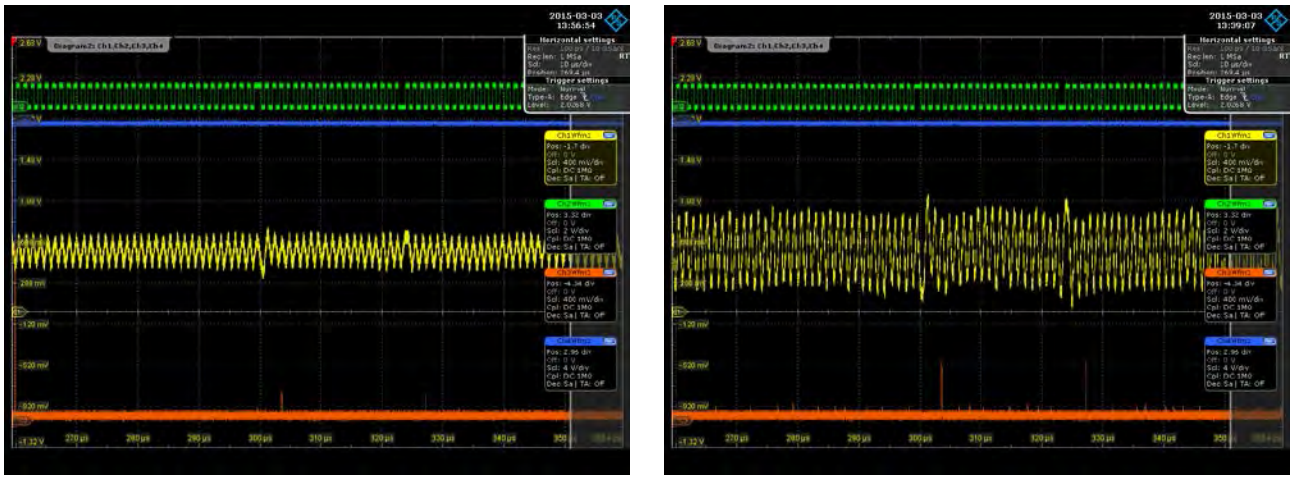
1. RxGain (CLIF_ANA_RX_REG) = 0…3

2. HPCF (CLIF_ANA_RX_REG) = 0…3
3. MIN_LEVEL (SIGPRO_RM_CONFIG1_REG) = 0…F
4. MIN_LEVEL_P (SIGPRO_RM_CONFIG1_REG) = 0…F

The effect of changing the RxGain in combination with HPCF can directly be seen in the unfiltered I or Q channel signal.

The Fig 46 shows the same test case with the same LMA level and the same bandwidth (HPCF), but just different settings for RxGain. On the left hand side the RxGain is set to 2, on the right hand side the RxGain is set to 3 (maximum). Both, Q channel signal and BPSK_SUM signal show higher signal level as well as higher noise level when using a higher RxGain.

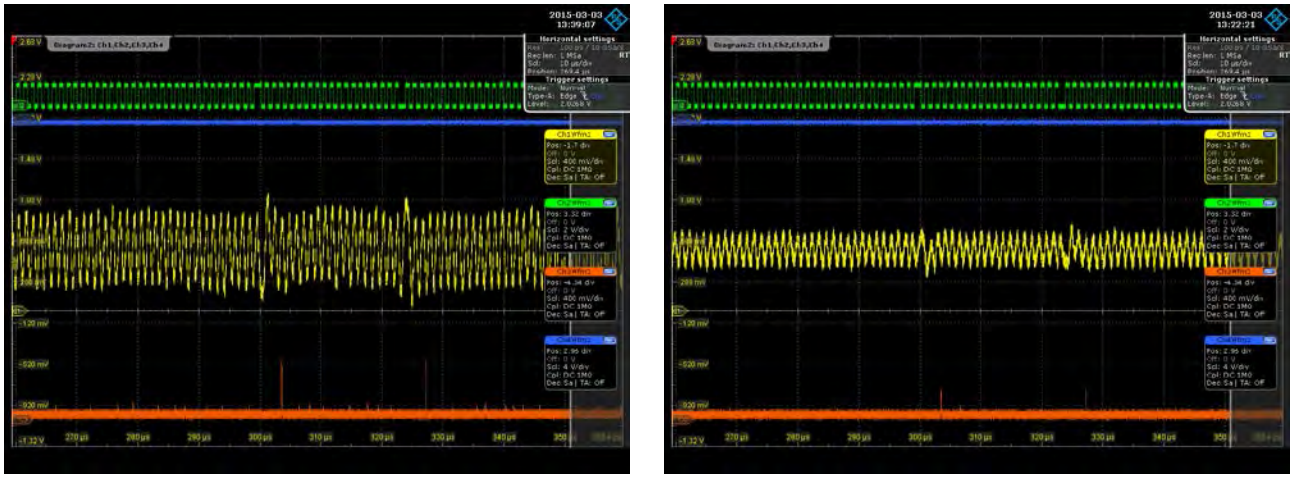
The Fig 47 shows the same test case with the same LMA level and the same RxGain, but different settings for HPCF. On the left hand side the HPCF is set to 0, on the right hand side the HPCF is set to 3 (maximum). Both, Q channel signal and BPSK_SUM signal show lower signal level as well as lower noise level when using a higher HPCF (i.e. a lower bandwidth).



a. RxGain = 2; HPCF = 0
b. Green: LMA (RefPICC input)
c. Blue: TX_ACTIVE (Trigger)
d. Yellow: unfiltered Q-Channel
e. Orange: BPSK_SUM

f. RxGain = 3; HPCF = 0
g. Green: LMA (RefPICC input)
h. Blue: TX_ACTIVE (Trigger)
i. Yellow: unfiltered Q-Channel
j. Orange: BPSK_SUM

Fig 46. Test signals for Type B, comparison of RxGain



a. RxGain = 3; HPCF = 0
b. Green: LMA (RefPICC input)
c. Blue: TX_ACTIVE (Trigger)
d. Yellow: unfiltered Q-Channel
e. Orange: BPSK_SUM

f. RxGain = 2; HPCF = 3
g. Green: LMA (RefPICC input)
h. Blue: TX_ACTIVE (Trigger)
i. Yellow: unfiltered Q-Channel
j. Orange: BPSK_SUM

Fig 47. Test signals for Type B, comparison of HPCF

Note: The RxGain should not be used with the maximum setting. The optimum performance can typically be found the RxGain = 2.

Note: The HPCF should typically be set to 0 for higher bit rates. For the standard bit rates (106 kbit/s) the HPCF of 2 or even 3 might improve the performance, especially under noisy environmental conditions.

MinLevel can be seen as a threshold value for the subcarrier signal on I and Q channel. The subcarrier signal must exceed the threshold to be taken into account by the PN7462AU decoder.

Note: The MinLevel is dynamically adapted inside the PN7462AU, i.e. with a very high level of subcarrier signal the Minlevel is automatically increased internally to increase the signal to noise ratio.

MinLevelP can be seen as a threshold for the decoded BPSK signal (BPSK_SUM). The BPSK signal must exceed the MinLevelP to be taken into account be the PN7462AU data decoder.

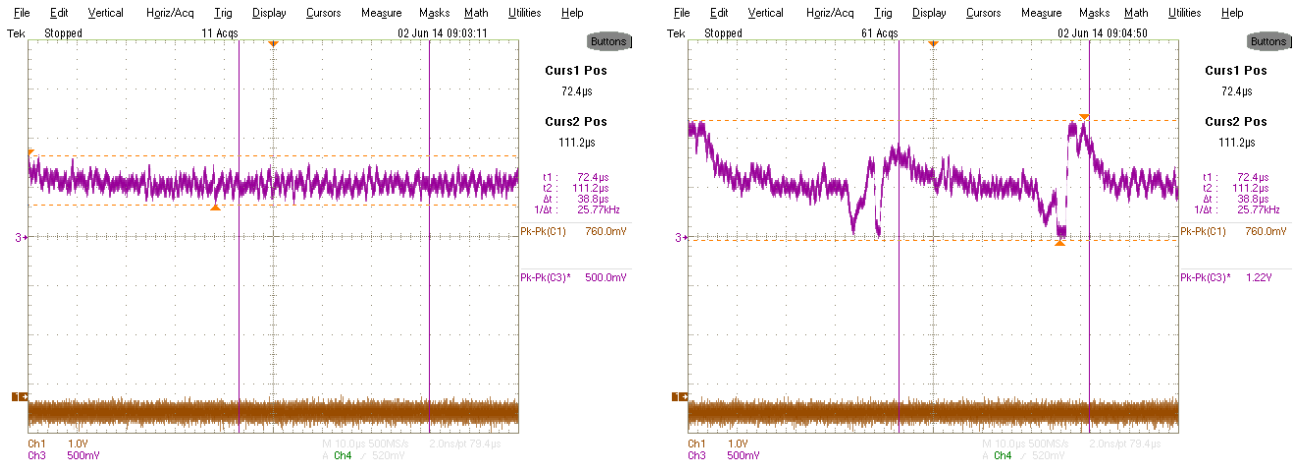
Note: The MinLevelP setting is not relevant for type A at 106kbit/s at all.

Note: The unfiltered I and Q channel signals are always present, while the filtered I and Q signals only apply when the Rx is active (RxActive).

4.6.3 Noise check

The Fig 48a shows a Q channel signal and the card response LMA (at the ReferencePICC input) using a type B setting without card response and without noise. The Fig 48b shows the same test case with the same settings, but in this case some external noise is coupled into the circuit.

The example as shown in Fig 48b and Fig 49b uses an LCD which is placed very closely to the antenna coil. The LCD driver generates current peaks which couple magnetically into the antenna coil.

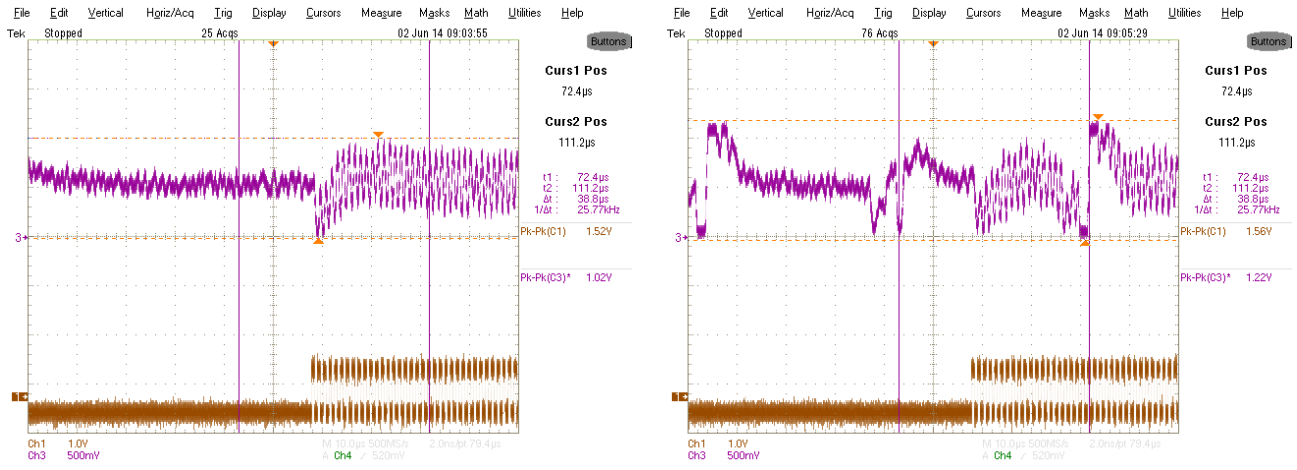


a. No card response, no noise

b. No card response, external noise

Fig 48. Type B without Card response

As you can see in Fig 49, the card response can be properly received in Fig 49a, where no noise applies. In Fig 49b the card response together with the noise is shown. The noise spikes, which are much larger than the sub carrier signal itself, introduce some clipping effects which are detected like phase shifts. This disturbs the type B communication. Such noise must be eliminated or at least reduced to a level which does not disturb the communication anymore.



a. Card response, no noise

b. Card response + noise

Fig 49. Type B with Card response

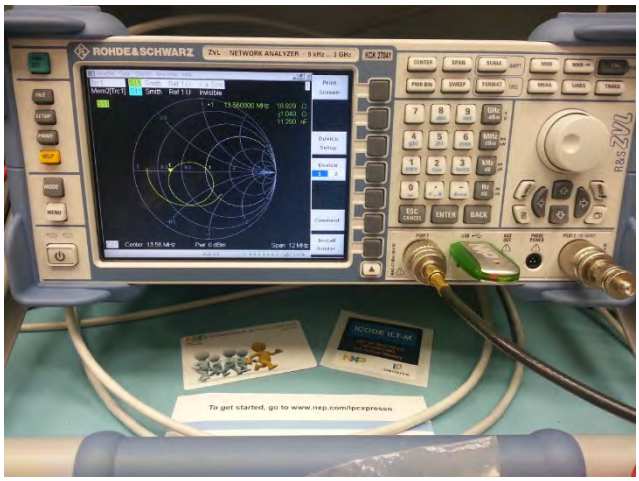
5. Annex

5.1 VNA and calibration

This annex describes some basics about impedance measurement and the related measurement tools.

5.1.1 Vector Network Analyzer

The impedance measurement must be done with a vector network analyzer, e.g. as shown in Fig 50.

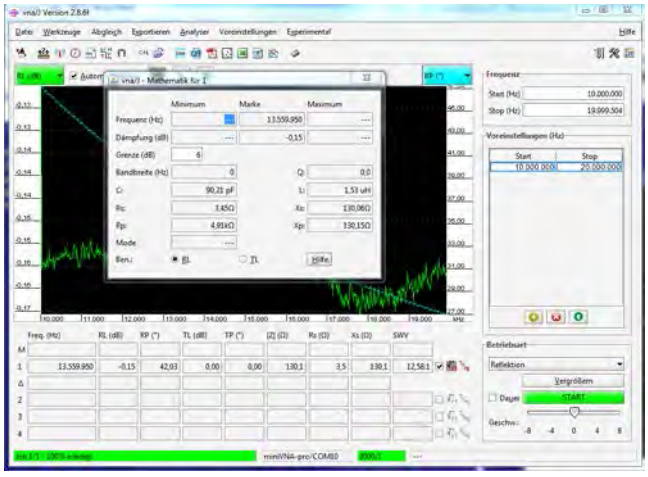


c. Rohde & Schwarz ZVL (refer to [11])

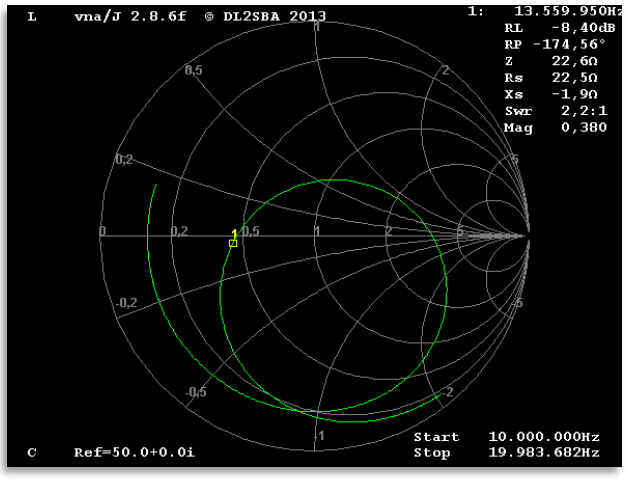
d. MiniVNA Pro (refer to [12])

Fig 50. Examples of Vector Network Analyzers

For the miniVNA Pro the recommendation is to use the VNA/J SW tool (refer to [13]), as shown in Fig 51.



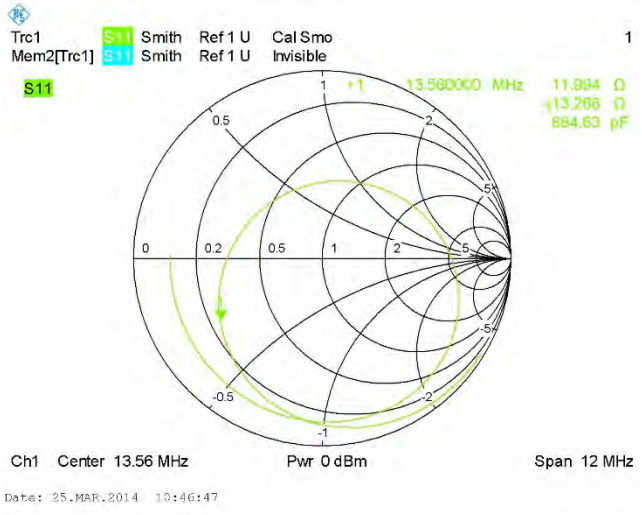
a. VNA/J with antenna coil measurement



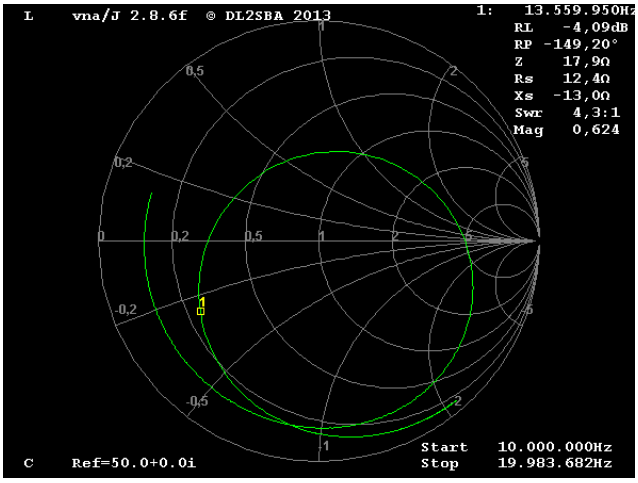
b. VNA/J Smith chart example

Fig 51. VNA/J from DL2SBA (refer to [13])

In Fig 52 the result of the same measurement is shown for the R&S ZVL as well as for the VNA/J using the miniVNAPro. The accuracy of the ZVL is much higher than the one of the miniVNA Pro. However, for the antenna matching and tuning procedure as described in this document, both devices can be used.



a. From R&S ZVL



b. From miniVNA Pro

Fig 52. Impedance Measurement result example (Smith chart)

5.1.2 Impedance measurement

The impedance measurement, which is needed to tune the antenna circuit correctly, is a S11 measurement, showing the normalized resistance and reactance of the antenna circuit impedance in a smith chart:

$$\underline{Z} = \underline{|Z|} \cdot e^{j\theta} = R + jX \quad (5)$$

$\underline{Z}$ = complex impedance

Θ = phase between voltage and current

R = real part, resistance

X = imaginary part, reactance

The smith chart shows the normalized impedance, typically normalized to 50Ω. Some measurement and simulation tools allow a normalization to values different than 50Ω. However, in this document the normalization is not changed.

The return loss (reflection coefficient), which can be directly derived from the S11 measurement (i.e. from the smith chart), is of no interest for the NFC Reader antenna tuning, since no 50Ω system is used. This return loss could only be used, if the chosen target impedance is 50Ω. Anyhow the return loss does not show the phase or whether the circuit is capacitive or inductive.

Typically a frequency sweep from 10MHz to 20MHz is sufficient enough to do the antenna tuning.

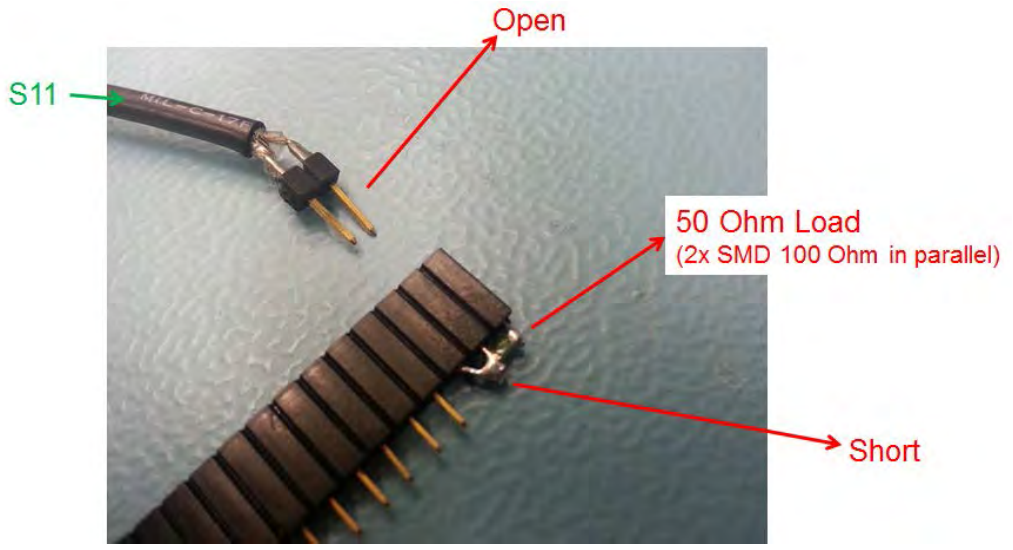
The standard VNA provides an unbalanced 50Ω measurement port, which is used here to measure a balanced impedance. The mismatch due to this setup error can be neglected.

The power level must be low enough (e.g. 0dBm or less), and the PN7462AU must be unpowered. Then the PN7462AU can remain in the circuit, while measuring the S11 between TX1 and TX2.

5.1.3 Calibration

The major part before the measurement itself is the calibration of the measurement tool (VNA) and measurement setup (cable and probe). A high end 50 Ω calibration kit for the used connector types (N-connector or SMA) does not help much, since the measurement itself needs to be done at the TX pins of the used NFC Reader IC as possible. Therefore the calibration must be done as close at these points as possible.

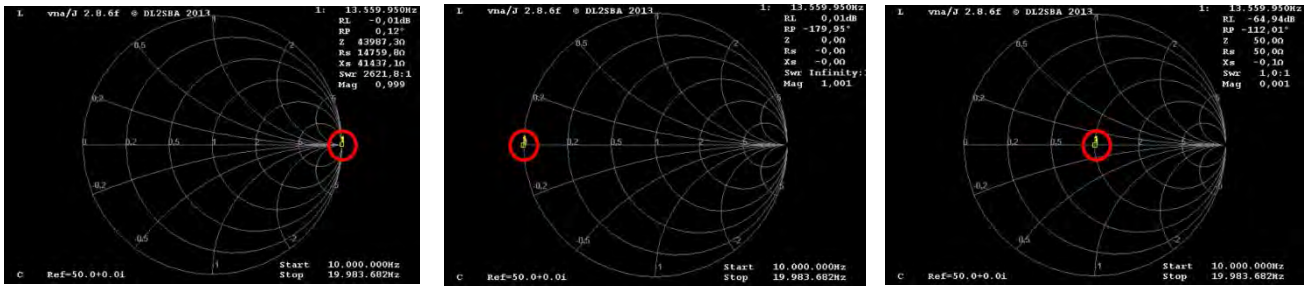
So the better solution is to create a simple connection, i.e. using a standard 2.54mm pin row connector (male and female) to connect the VNA. This can be used to measure the antenna impedance at the correct points, but also to calibrate the VNA. A very simple but highly efficient homemade connector and tool is shown in Fig 53.



(1) The mismatch due to the unbalanced measurement of a balanced impedance can be ignored.

Fig 53. Measurement connector and calibration kit

After the calibration the measurement setup should be checked and should show the results as shown in Fig 54.



a. Open b. Short c. Load

Fig 54. Calibration result

5.2 Toolchain for register change

The following part describes the toolchain that is needed to change and optimize the register settings.

5.2.1 Software

- LPCxpresso environment V7.6 and above
- Plugin for CLIF register access (com.nxp.pn640.update-7.6.0-SNAPSHOT-110)
- Software example that allows register changes during the execution (PN7462AU_ex_phExRf_Polling)

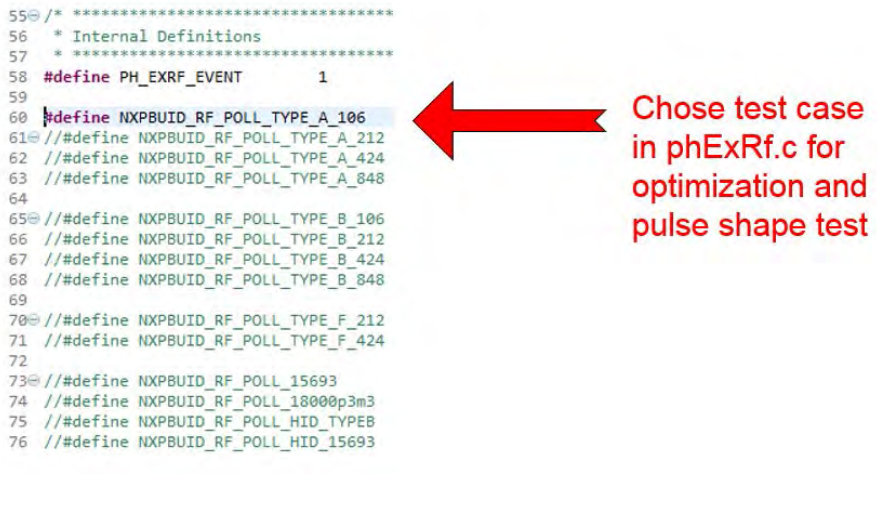
For further information on how to setup the tool chain refer to customer board UM.

5.2.2 How to change a register using the example code

This part describes how to change a register by using the PN7462AU_ex_phExRf_Polling example.

For further information on how to import a project refer to customer board UM.

1) First step is to choose the communication standard and bitrate that needs to be optimized. This is done by uncomment the targeted standard in the phExRf.c.



(1) Defines in phExRf.c

Fig 55. Defines for setting the communication standard

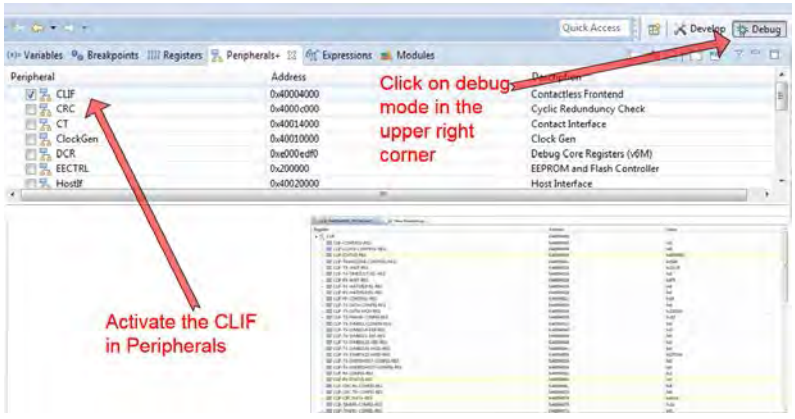
2) Debug PN7462AU_ex_phExRf_Polling.

3) Place breakpoint while example is running in the corresponding phExRf_xxxx.c file. This breakpoint needs to be in the while loop as shown in Fig 56. This needs to be done to pause the example while the endless polling is performed. If the example is paused the registers can be changed.

(1)

Fig 56. Placing breakpoint to pause example to change register

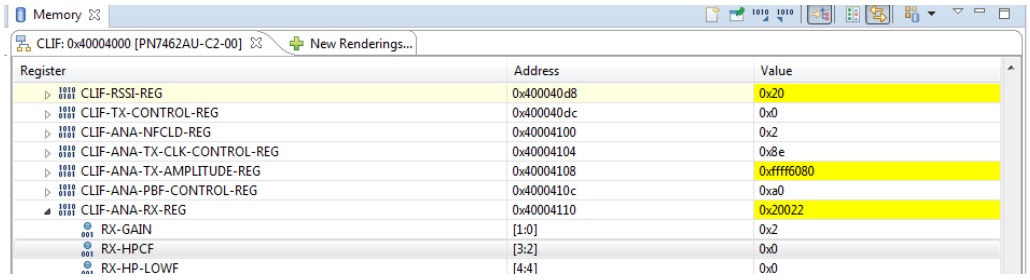
4) Change the view mode in LPCxpresso to Debug (Fig 57).



(1)

Fig 57. Changing to debug mode in LPCxpresso view

5) Change register value. The register value can be changed in the memory section of the LPCxpresso environment (Debug view Fig 58). After the register is changed remove the breakpoint and resume the example.



(1)

Fig 58. Changing CLIF registers in debug mode

6. References

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Date of release: 9 March 2016
336910
Document identifier: AN11706